OIPE JC133
OCT 22 2004
PATENT & TRADEMARK OFFICE

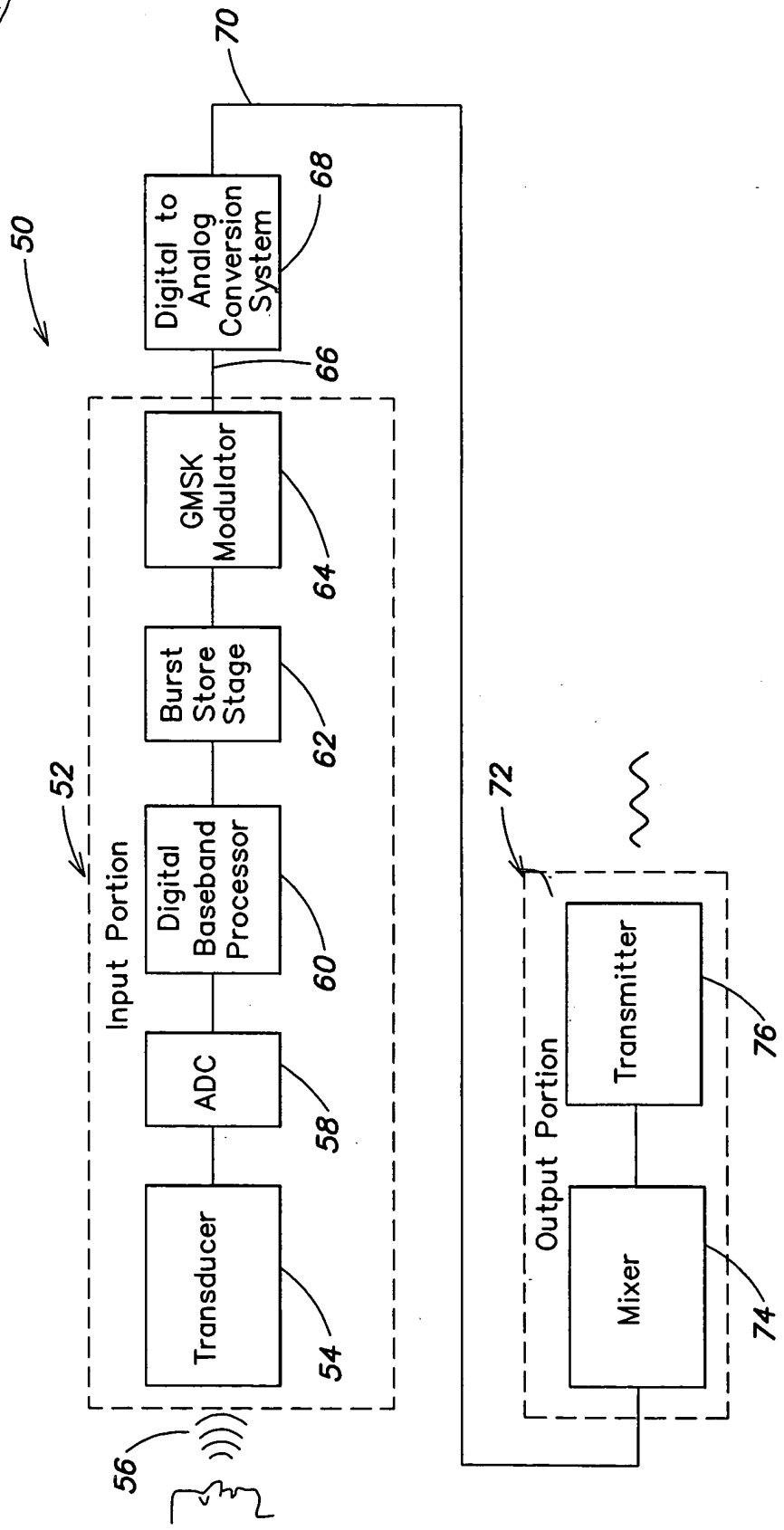


FIG. 1

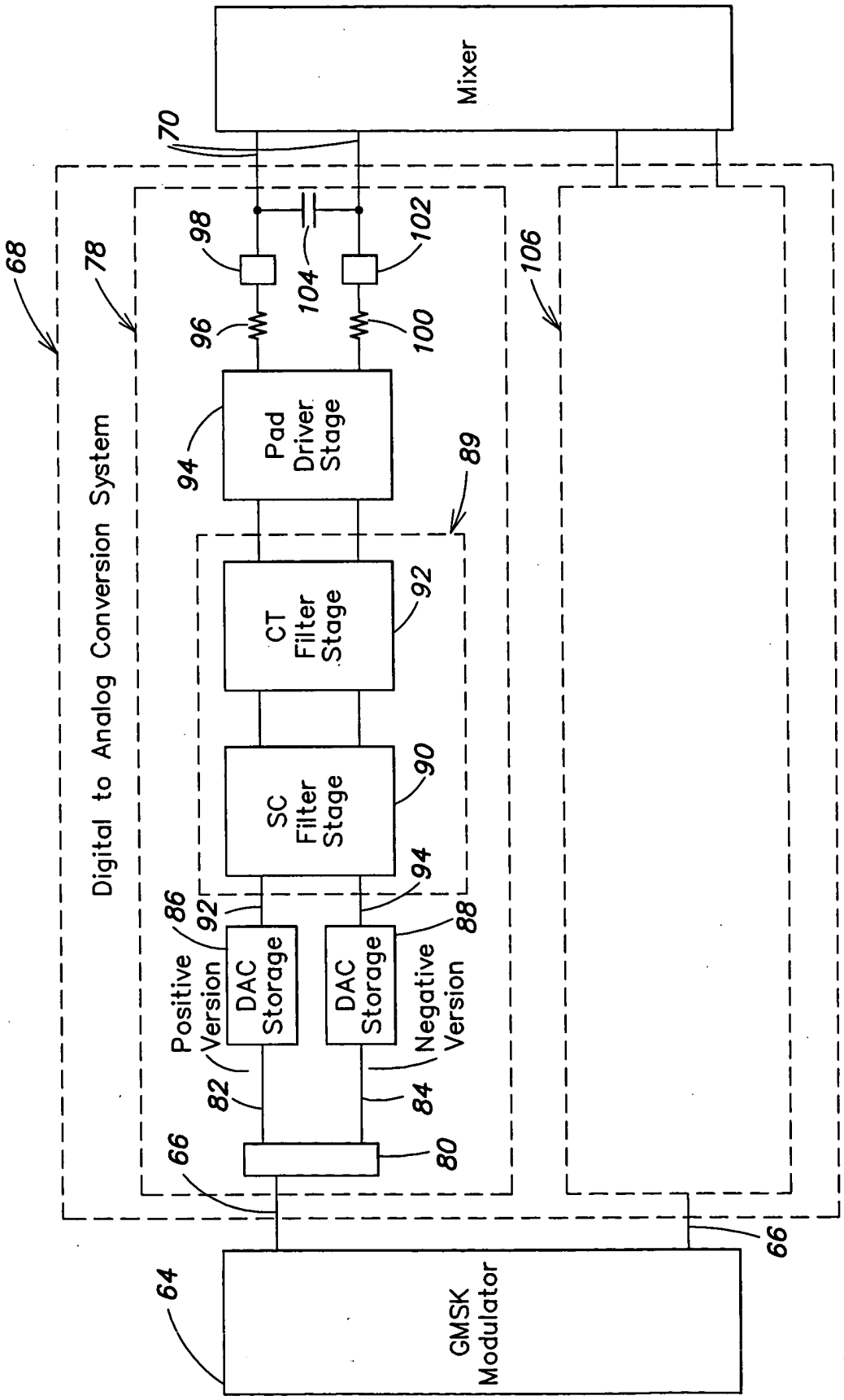

Mixer
70
68
78
106
98
102
104
96
100
Pad Driver Stage
94
89
CT Filter Stage
92
SC Filter Stage
90
94
86
92
88
Positive Version
DAC Storage
DAC Storage
Negative Version
82
84
80
66
66
64
GMSK Modulator
Digital to Analog Conversion System

FIG. 2

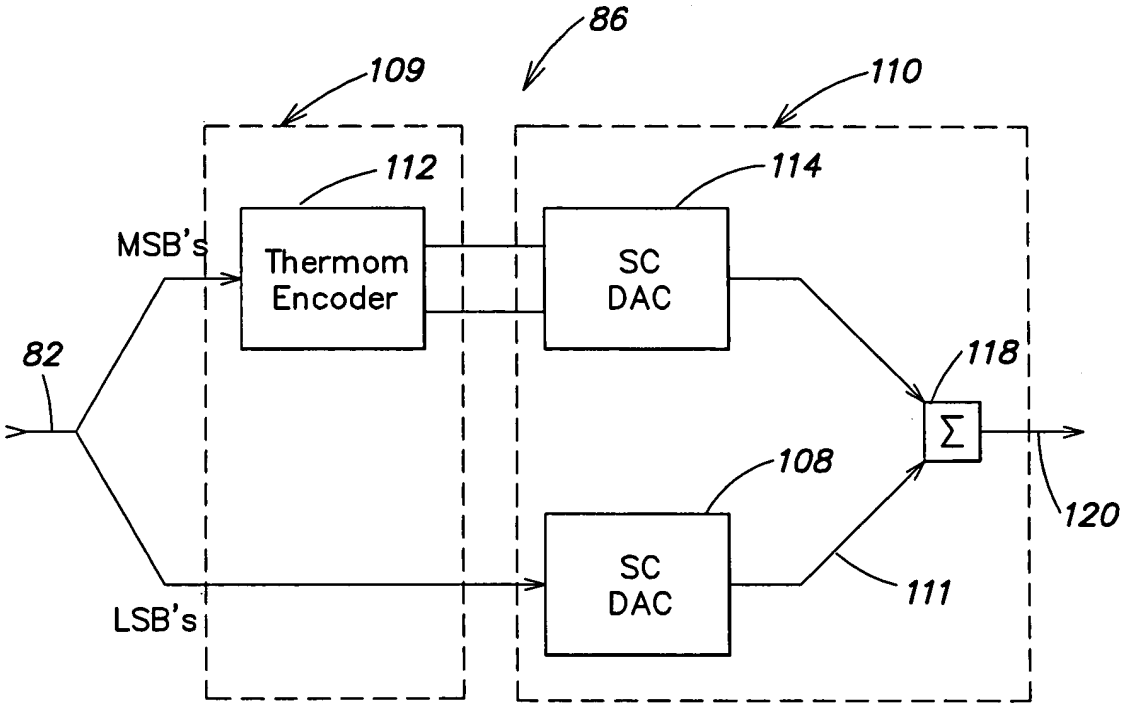

86
109
110
112
114
MSB's
Thermom
Encoder
SC
DAC
82
118
Σ
108
120
SC
DAC
111
LSB's

FIG. 3

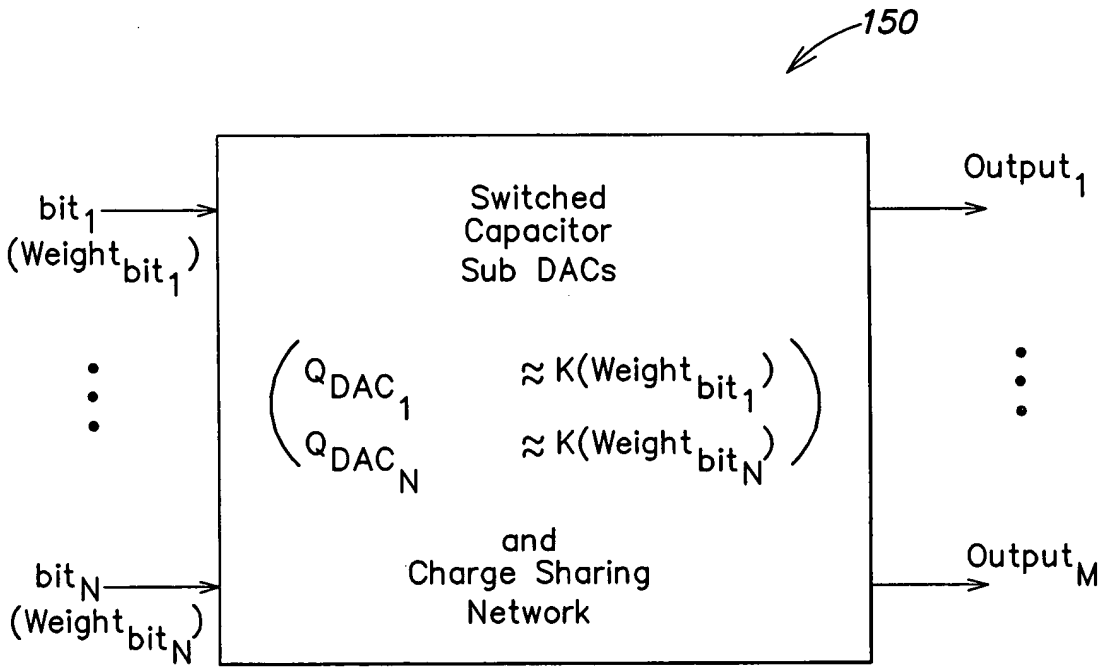

150
bit 1
(Weight bit 1)
bit N
(Weight bit N)
Switched
Capacitor
Sub DACs
Q DAC 1 ≈ K(Weight bit 1)
Q DAC N ≈ K(Weight bit N)
and
Charge Sharing
Network
Output 1
Output M

FIG. 4

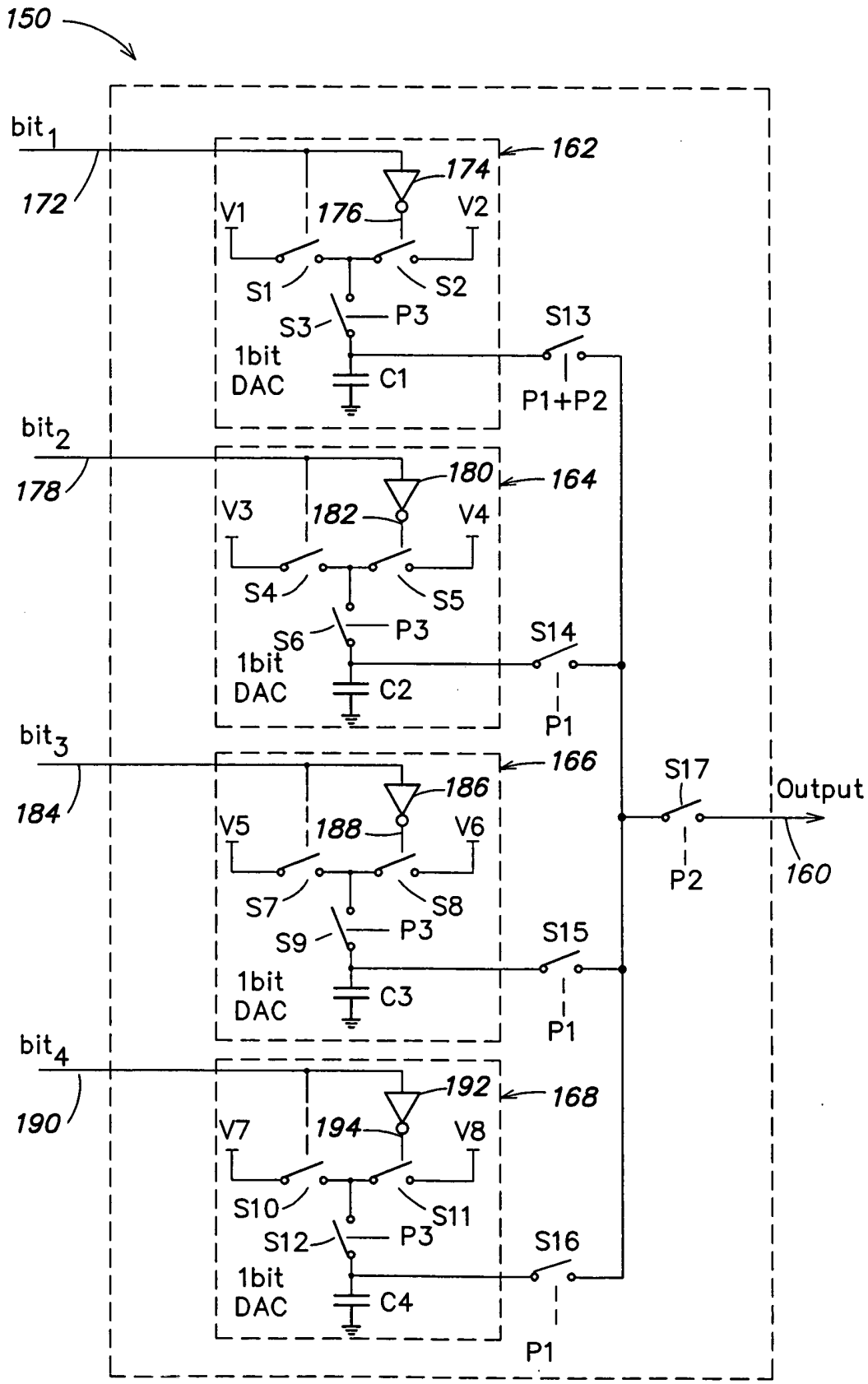

150
bit1
172
162
174
V1
176
V2
S1
S2
S3
P3
S13
1bit
DAC
C1
P1+P2
bit2
178
164
180
V3
182
V4
S4
S5
S6
P3
S14
1bit
DAC
C2
P1
bit3
184
166
186
V5
188
V6
S7
S8
S9
P3
S15
1bit
DAC
C3
P1
S17
Output
P2
160
bit4
190
168
192
V7
194
V8
S10
S11
S12
P3
S16
1bit
DAC
C4
P1

FIG. 5

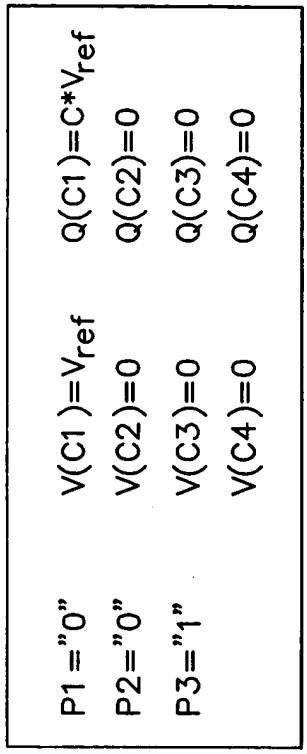
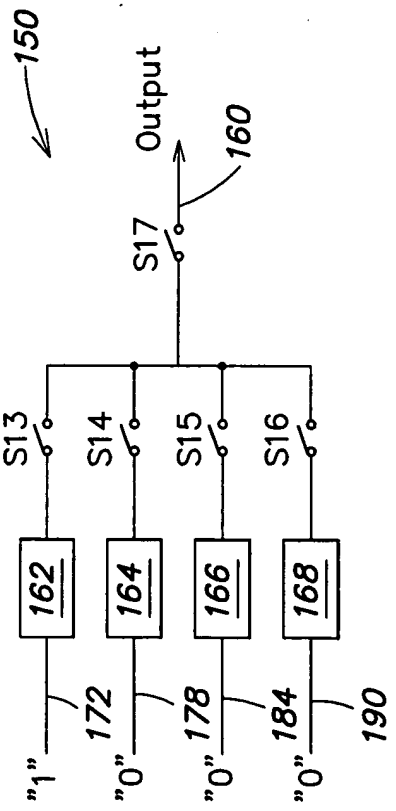

P1 = "0"
P2 = "0"
P3 = "1"
V(C1)=Vref
V(C2)=0
V(C3)=0
V(C4)=0
Q(C1)=C*Vref
Q(C2)=0
Q(C3)=0
Q(C4)=0

FIG. 7A


150
Output
160
S17
S13
S14
S15
S16
162
164
166
168
"1"
"0"
"0"
"0"
172
178
184
190

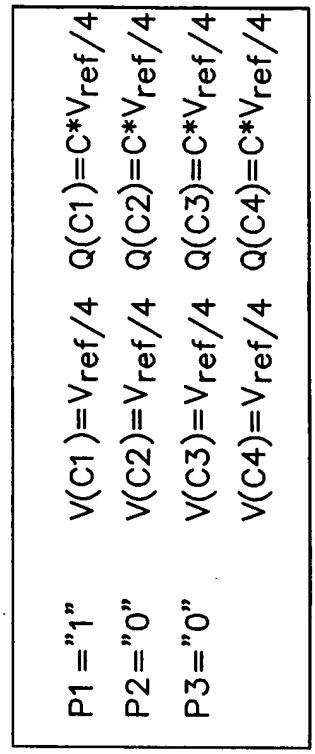
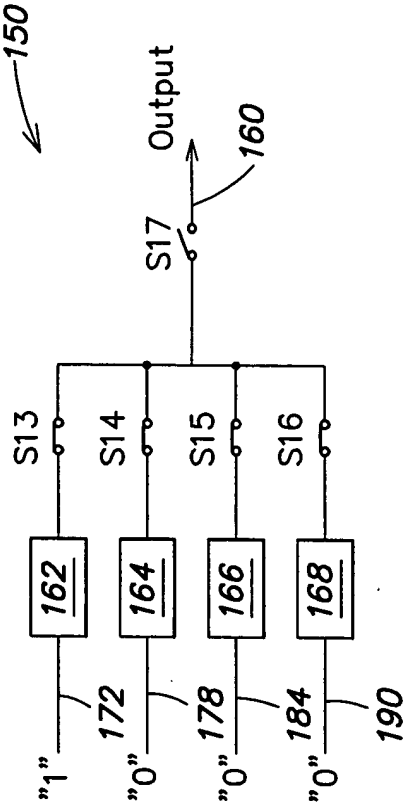
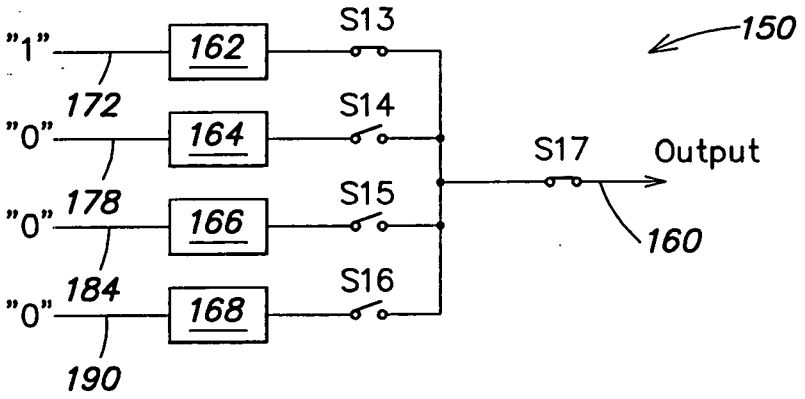

P1 = "1"
P2 = "0"
P3 = "0"
V(C1)=Vref/4
V(C2)=Vref/4
V(C3)=Vref/4
V(C4)=Vref/4
Q(C1)=C*Vref/4
Q(C2)=C*Vref/4
Q(C3)=C*Vref/4
Q(C4)=C*Vref/4

FIG. 7B


150
Output
160
S17
S13
S14
S15
S16
162
164
166
168
"1"
"0"
"0"
"0"
172
178
184
190



P1 ="0"	$V(C1)=V_{ref/4}$	$Q(C1)=C*V_{ref/4}$
P2="1"	$V(C2)=V_{ref/4}$	$Q(C2)=C*V_{ref/4}$
P3="0"	$V(C3)=V_{ref/4}$	$Q(C3)=C*V_{ref/4}$
	$V(C4)=V_{ref/4}$	$Q(C4)=C*V_{ref/4}$

FIG. 7C

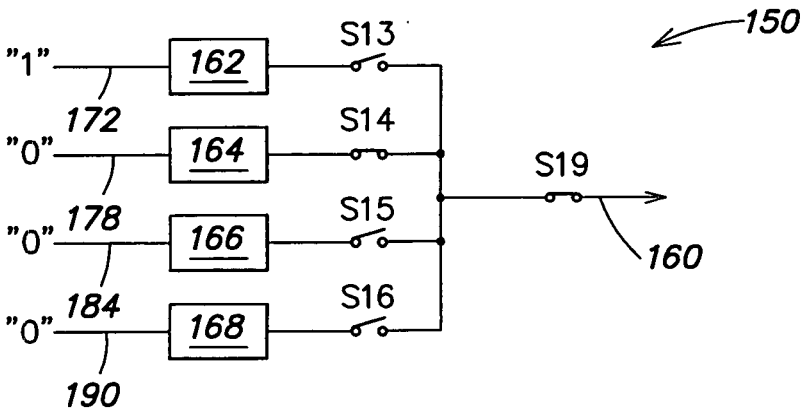


FIG. 10

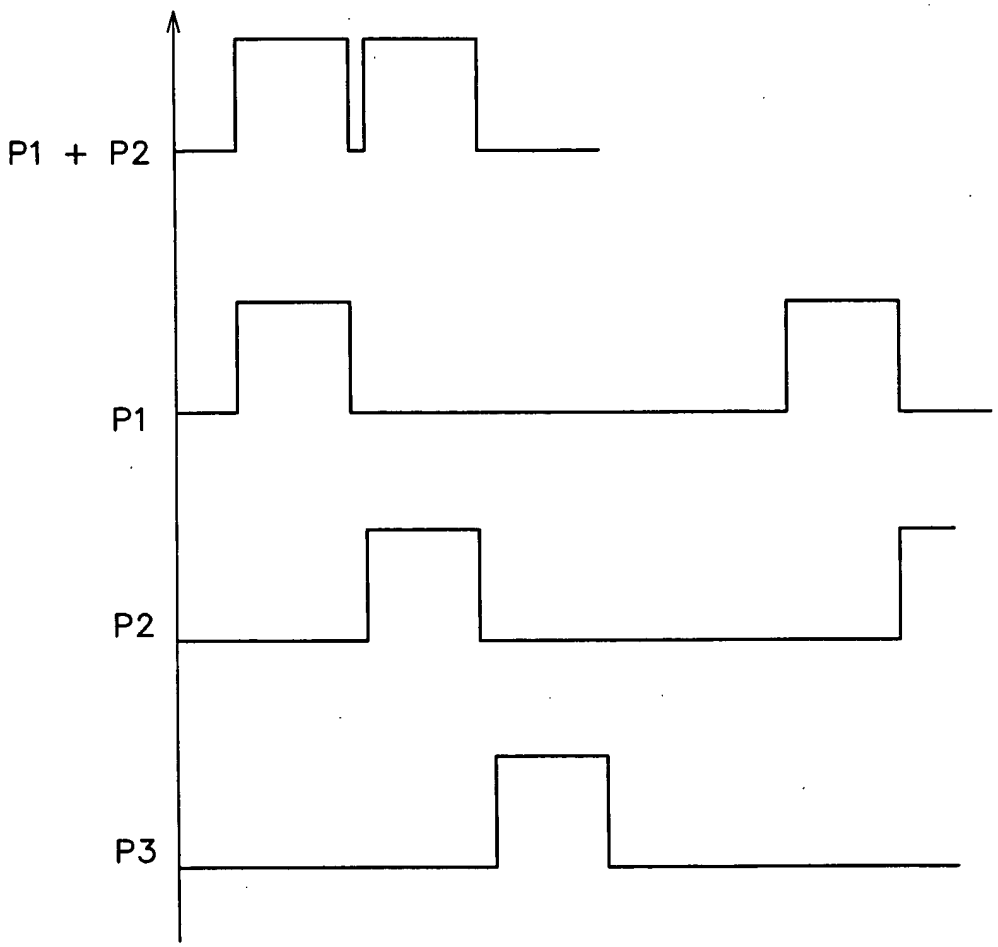
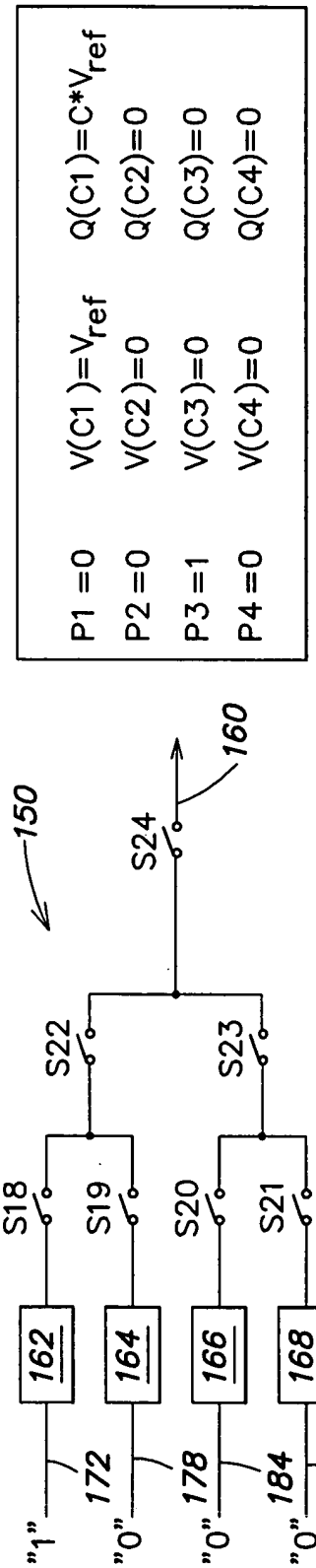
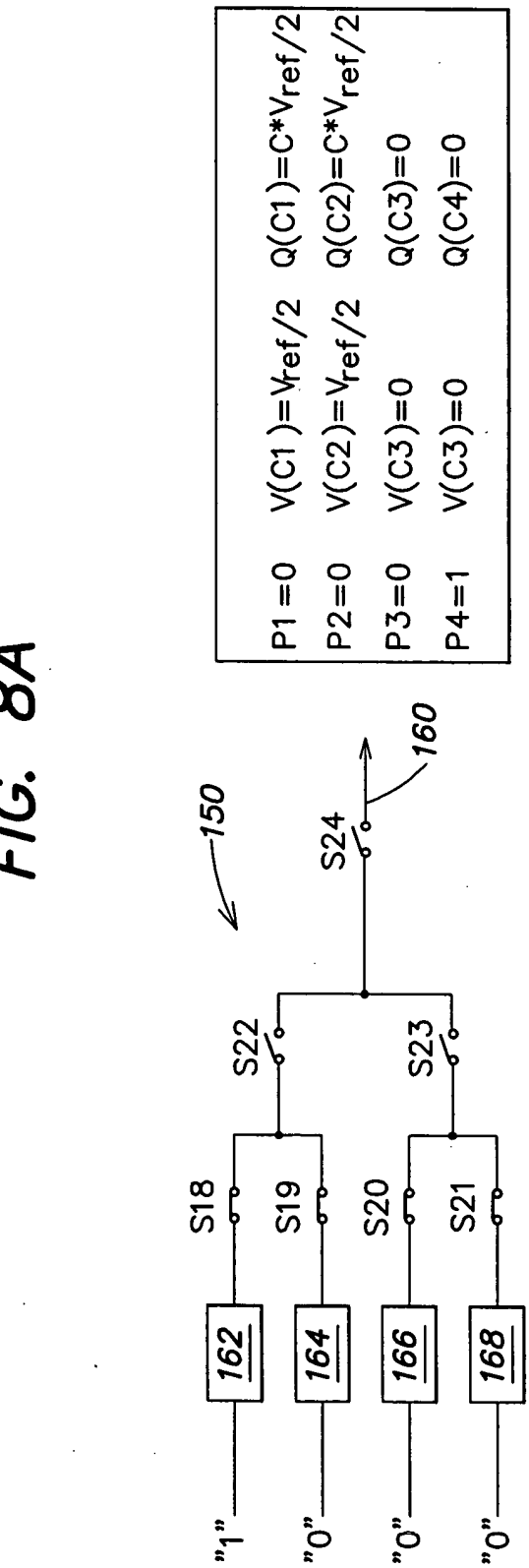


FIG. 6



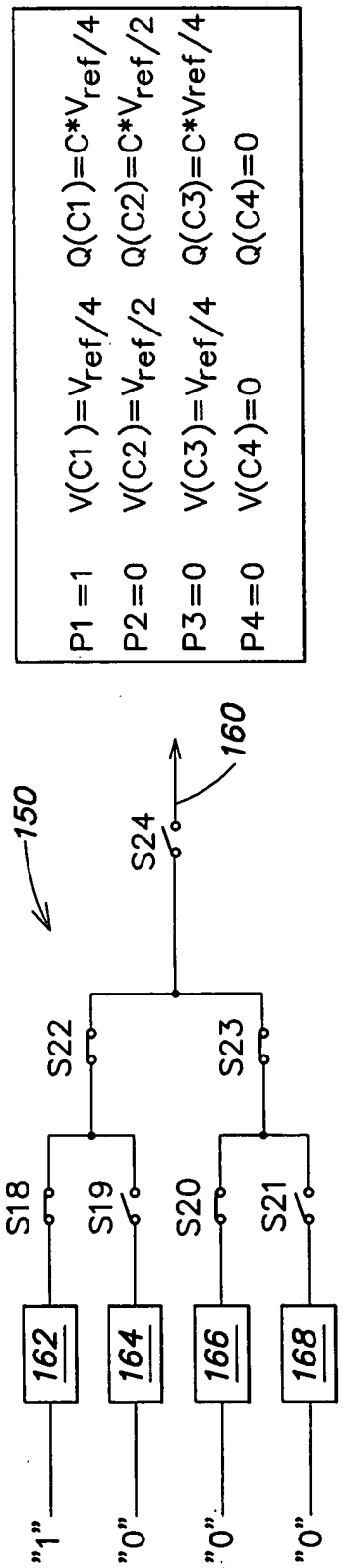
P1 =0	V(C1)=V_{ref}	Q(C1)=C*V_{ref}
P2 =0	V(C2)=0	Q(C2)=0
P3 =1	V(C3)=0	Q(C3)=0
P4 =0	V(C4)=0	Q(C4)=0

FIG. 8A



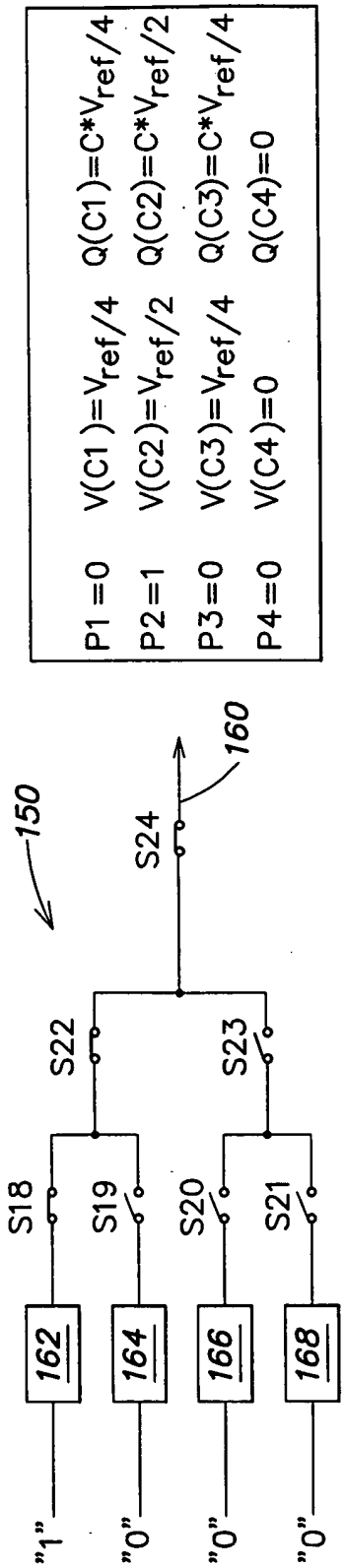
P1 =0	V(C1)=Vref/2	Q(C1)=C*Vref/2
P2=0	V(C2)=Vref/2	Q(C2)=C*Vref/2
P3=0	V(C3)=0	Q(C3)=0
P4=1	V(C3)=0	Q(C4)=0

FIG. 8B



P1 =1	V(C1)=V_{ref}/4	Q(C1)=C*V_{ref}/4
P2=0	V(C2)=V_{ref}/2	Q(C2)=C*V_{ref}/2
P3=0	V(C3)=V_{ref}/4	Q(C3)=C*Vref/4
P4=0	V(C4)=0	Q(C4)=0

FIG. 8C



P1 =0	V(C1)=V_{ref}/4	Q(C1)=C*V_{ref}/4
P2=1	V(C2)=V_{ref}/2	Q(C2)=C*V_{ref}/2
P3=0	V(C3)=V_{ref}/4	Q(C3)=C*V_{ref}/4
P4=0	V(C4)=0	Q(C4)=0

FIG. 8D

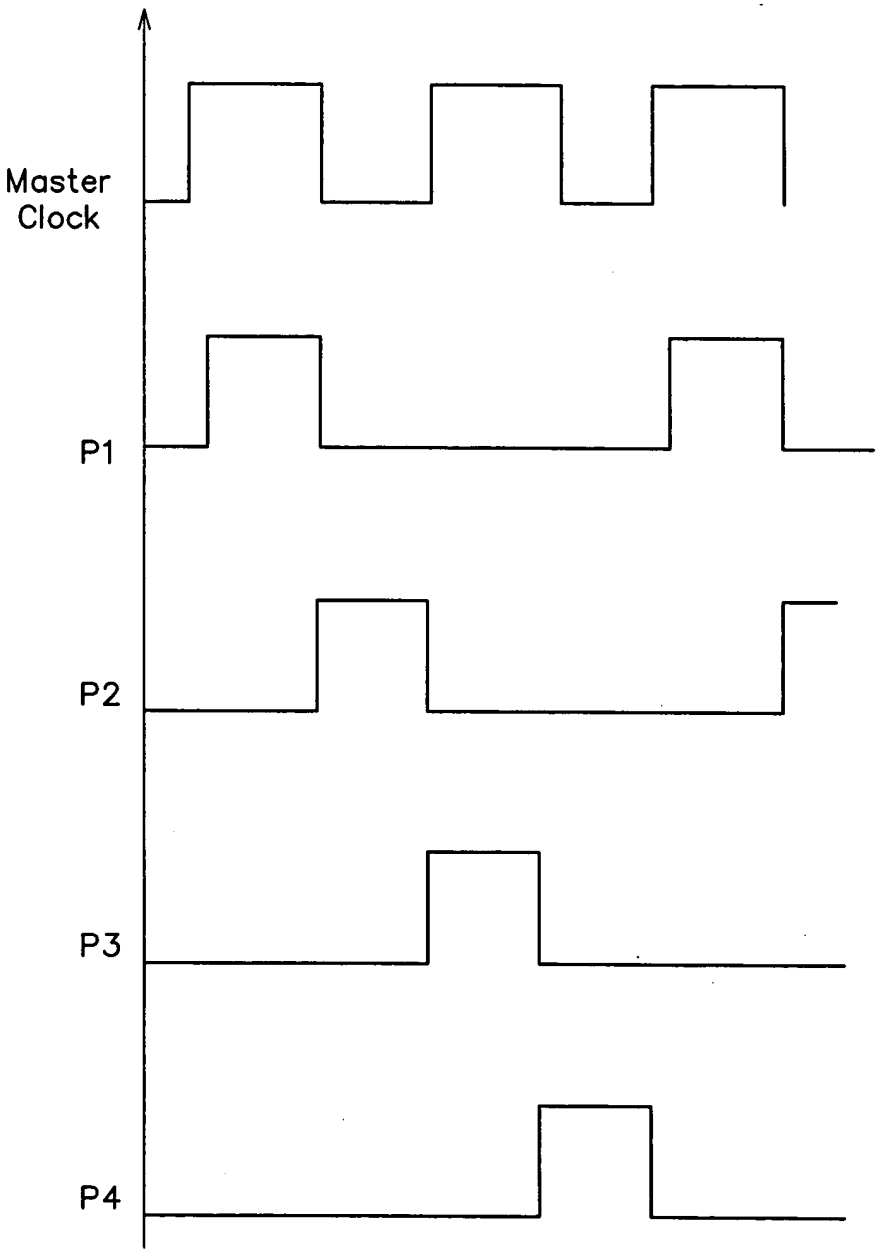


FIG. 9

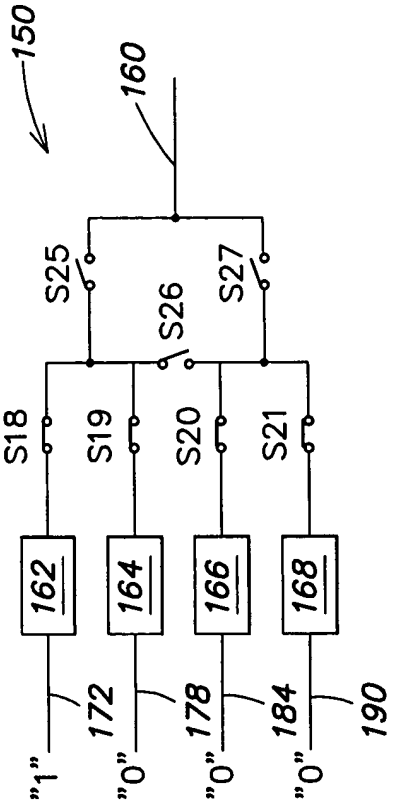


FIG. 11B

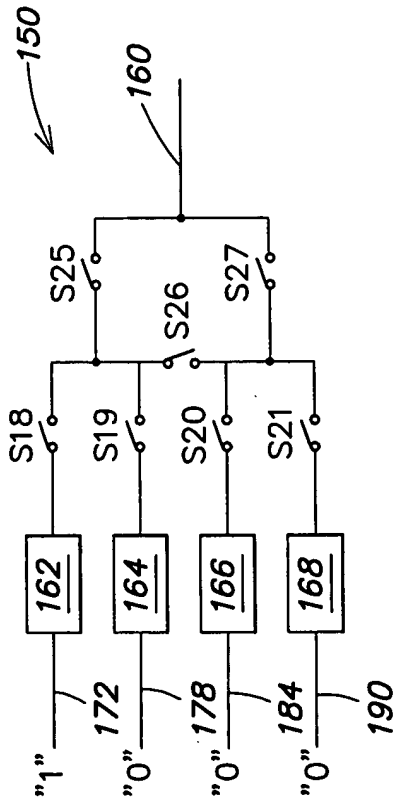


FIG. 11A

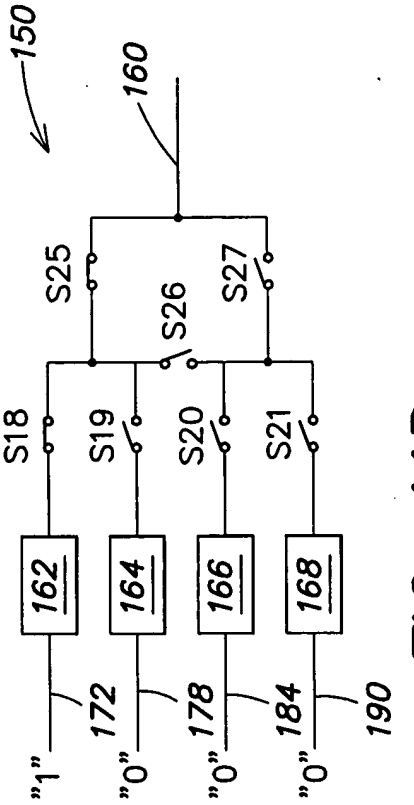


FIG. 11D

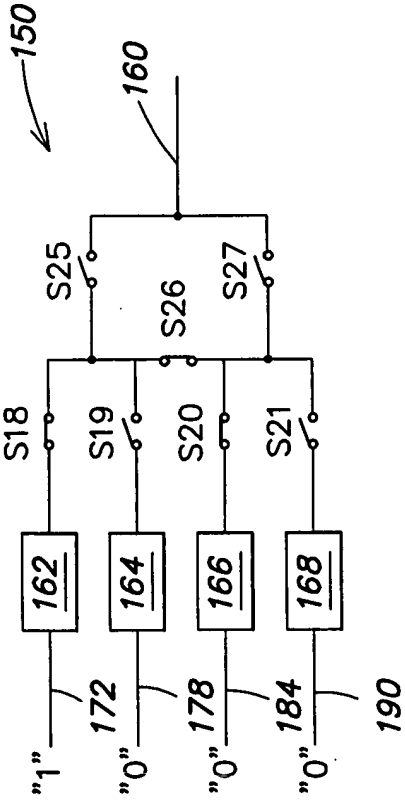
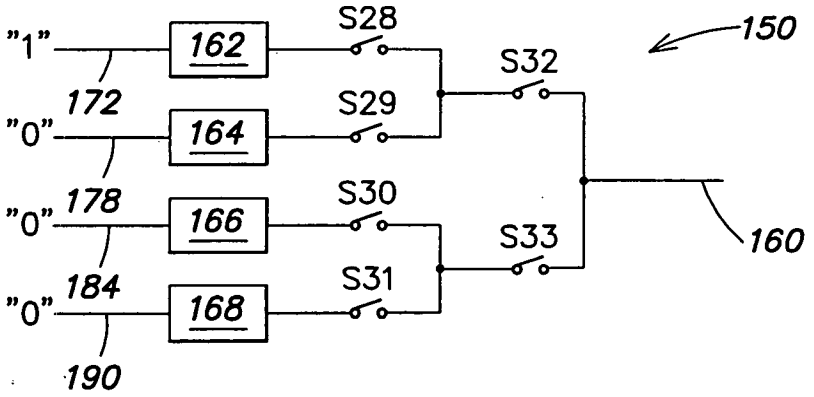
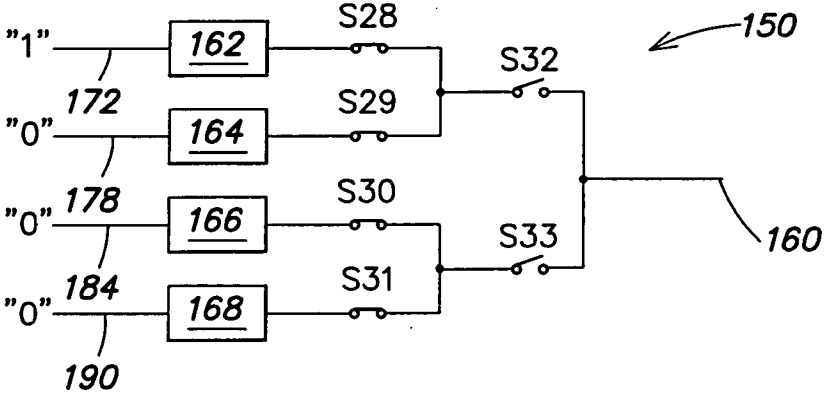


FIG. 11C



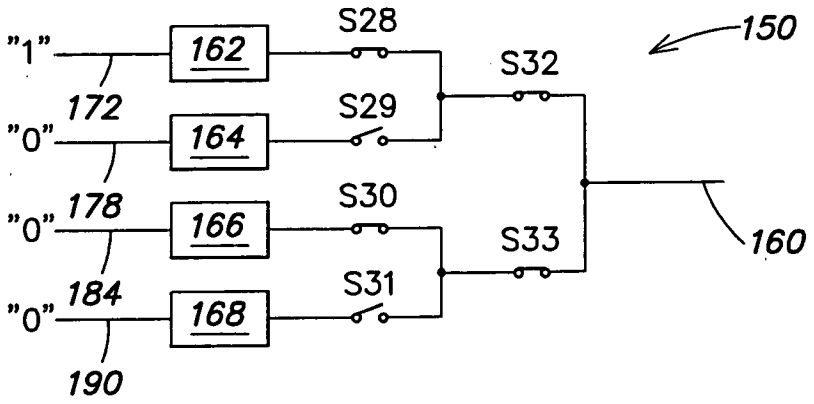
P1 =0	$V(C1)=V_{ref}$	$Q(C1)=C*V_{ref}$
P2 =0	V(C2)=0	Q(C2)=0
P3 =1	V(C3)=0	Q(C3)=0
	V(C4)=0	Q(C4)=0

FIG. 12A



P1 =1	$V(C1)=V_{ref/2}$	$Q(C1)=C*V_{ref/2}$
P2=0	$V(C2)=V_{ref/2}$	$Q(C2)=C*V_{ref/2}$
P3=0	V(C3)=0	Q(C3)=0
	V(C4)=0	Q(C4)=0

FIG. 12B



P1 =0	$V(C1)=V_{ref/2}$	$Q(C1)=C*V_{ref/2}$
P2=1	$V(C2)=V_{ref/2}$	$Q(C2)=C*V_{ref/2}$
P3=0	V(C3)=0	Q(C3)=0
	V(C4)=0	Q(C4)=0

FIG. 12C

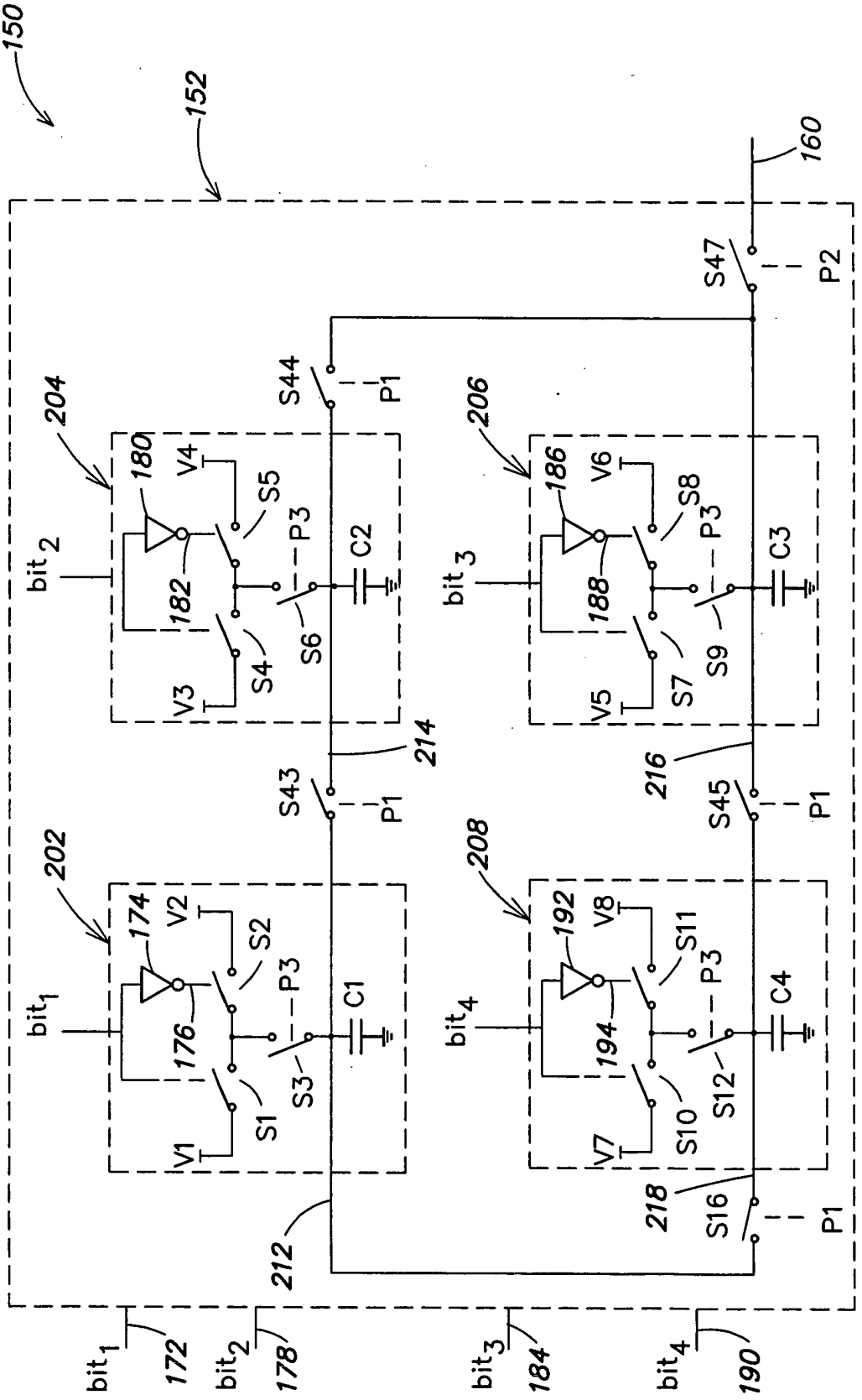
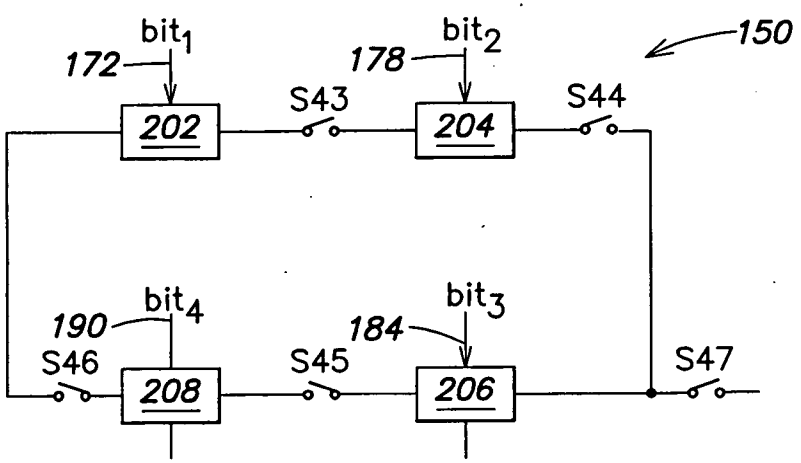
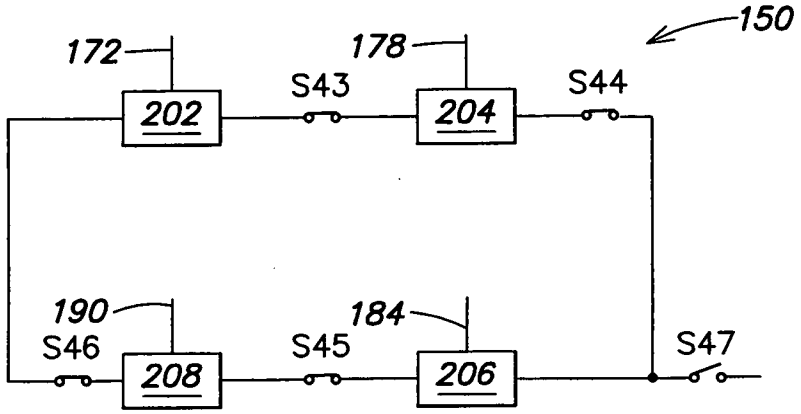

150
152
160
204
206
202
208
214
216
212
218
bit1
bit2
bit3
bit4
172
178
184
190
174
176
180
182
186
188
192
194
V1
V2
V3
V4
V5
V6
V7
V8
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S16
S43
S44
S45
S47
P1
P2
P3
C1
C2
C3
C4

FIG. 13



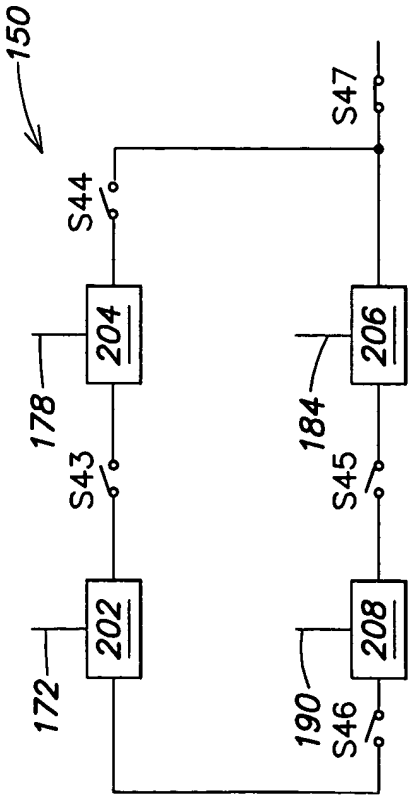
P1 =0 V(C1)=V_{ref} Q(C1)=C*V_{ref}
P2=0 V(C2)=0 Q(C2)=0
P3=1 V(C3)=0 Q(C3)=0
V(C4)=0 Q(C4)=0

FIG. 14A



P1=1 V(C1)=$V_{ref/4}$ Q(C1)=C*$V_{ref/4}$
P2=0 V(C2)=$V_{ref/4}$ Q(C2)=C*$V_{ref/4}$
P3=0 V(C3)=$V_{ref/4}$ Q(C3)=C*$V_{ref/4}$
V(C4)=$V_{ref/4}$ Q(C4)=C*$V_{ref/4}$

FIG. 14B



P1 =0 V(C1)=$V_{ref}/4$ Q(C1)=C*$V_{ref}/4$
P2 =1 V(C2)=$V_{ref}/4$ Q(C2)=C*$V_{ref}/4$
P3 =0 V(C3)=$V_{ref}/4$ Q(C3)=C*$V_{ref}/4$
V(C4)=$V_{ref}/4$ Q(C4)=C*$V_{ref}/4$

FIG. 14C

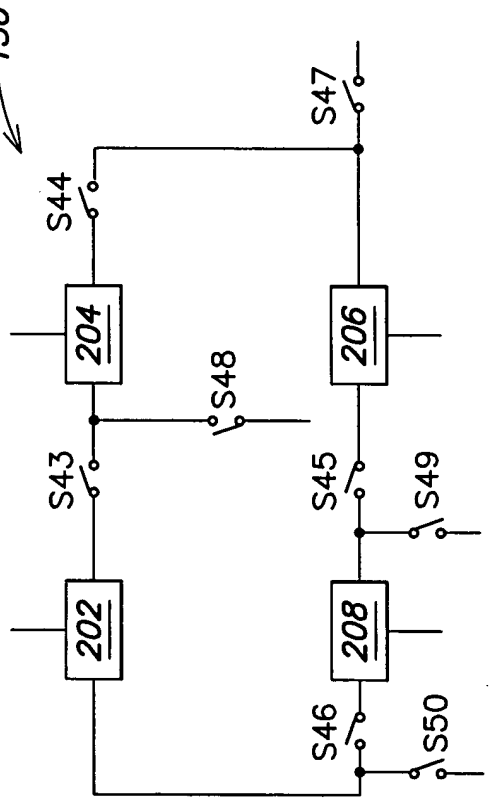


FIG. 15

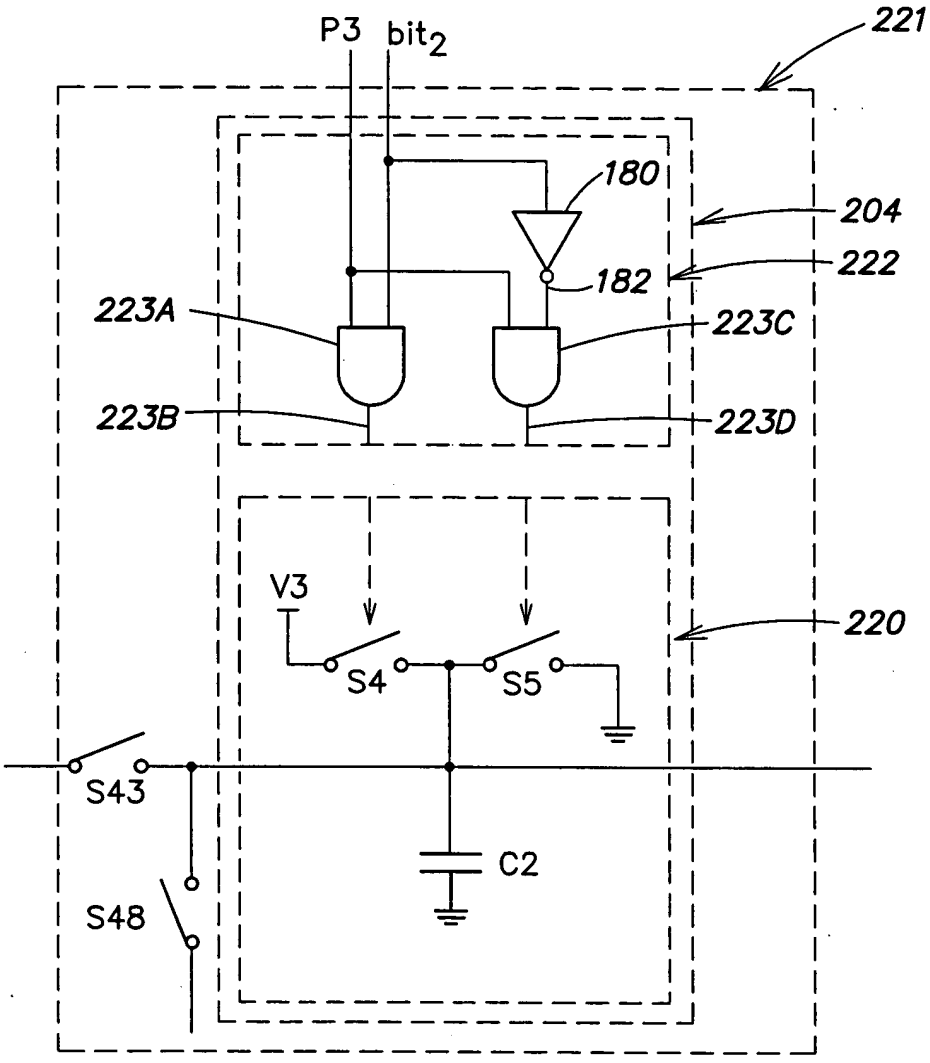

P3
bit2
221
180
204
222
182
223A
223C
223B
223D
V3
220
S4
S5
S43
C2
S48

FIG. 16A

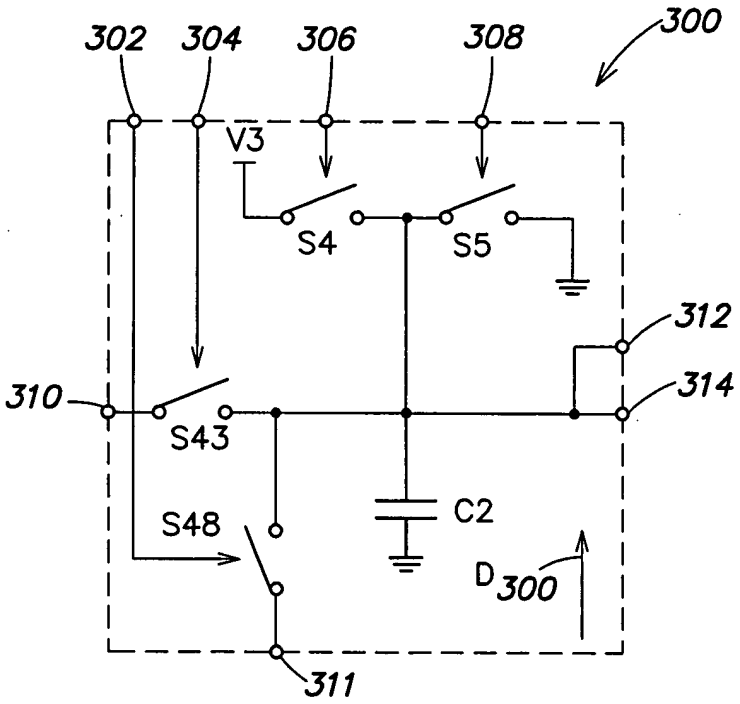


FIG. 16B

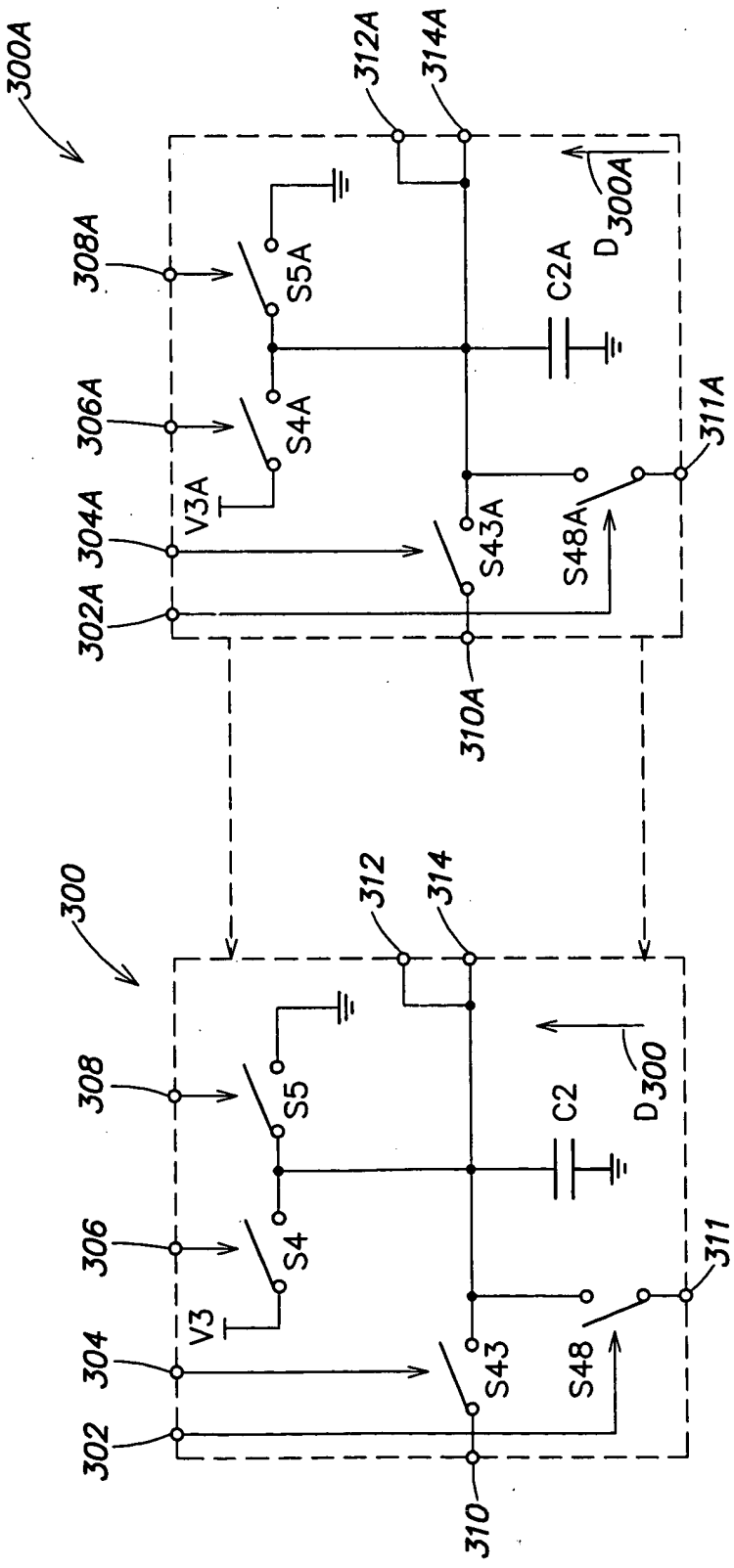

300A
312A
314A
308A
S5A
C2A
D300A
306A
S4A
311A
V3A
304A
S43A
S48A
302A
310A
300
312
314
308
S5
C2
D300
306
S4
311
V3
304
S43
S48
302
310

FIG. 16C

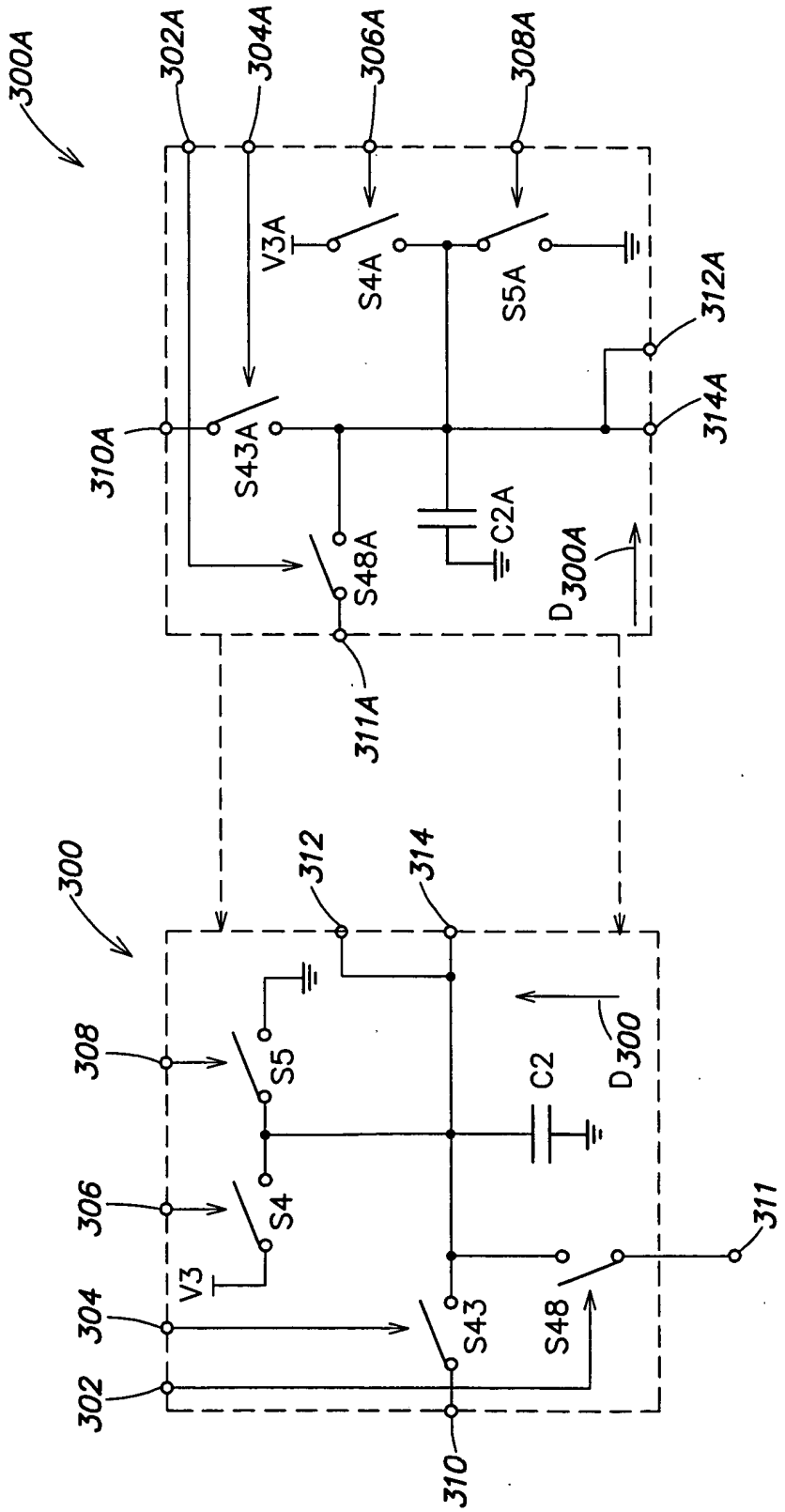

300A
302A
304A
306A
308A
V3A
S4A
S5A
312A
314A
310A
S43A
S48A
C2A
D300A
311A
300
312
314
308
S5
C2
D300
306
S4
V3
304
S43
S48
311
302
310

FIG. 16D

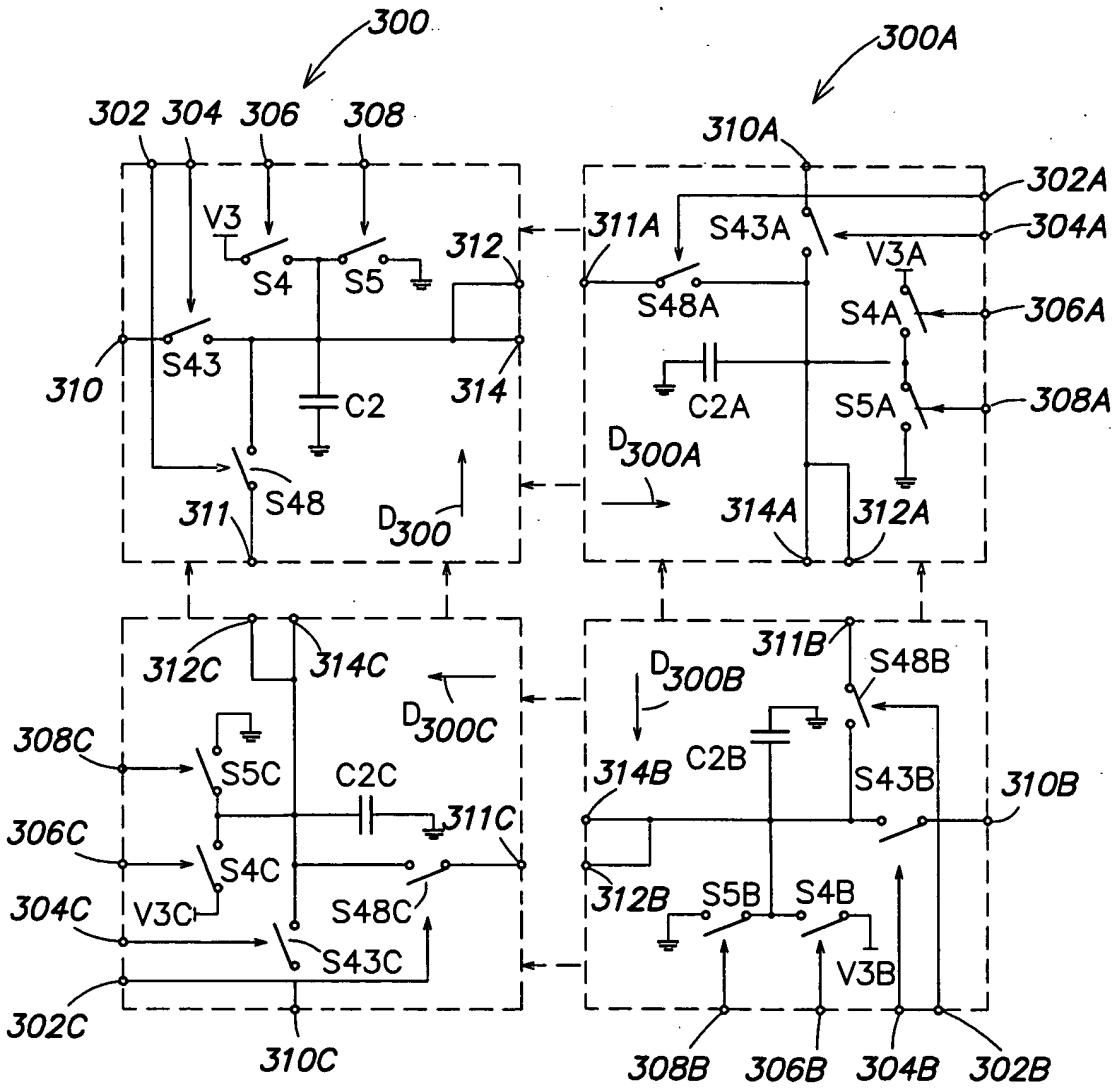

300
300A
302 304 306 308
310A
302A
304A
306A
308A
V3
S4
S5
312
311A
S43A
V3A
S48A
S4A
S43
310
314
C2
C2A
S5A
S48
311
D300
D300A
314A
312A
312C
314C
D300C
311B
D300B
S48B
308C
S5C
C2C
C2B
314B
S43B
310B
306C
S4C
311C
312B
S5B
S4B
304C
V3C
S48C
S43C
V3B
302C
310C
308B
306B
304B
302B

FIG. 16E

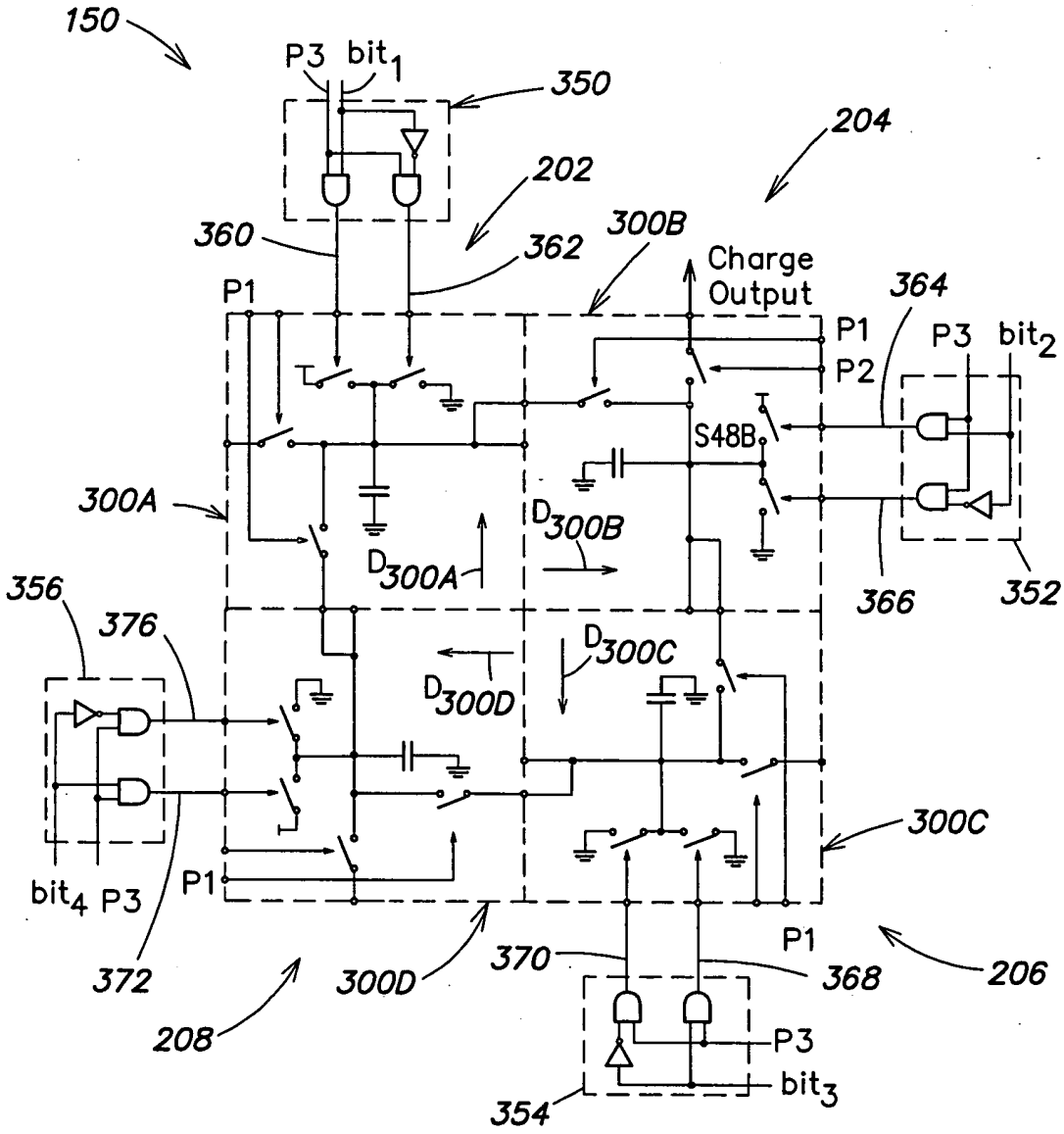

150
P3 bit1
350
204
202
360
362
300B
Charge Output
364
P1
P1
P2
P3 bit2
S48B
300A
D300B
D300A
356
376
366
352
D300C
D300D
300C
bit4 P3
P1
372
208
300D
370
P1
368
206
P3
bit3
354

FIG. 17

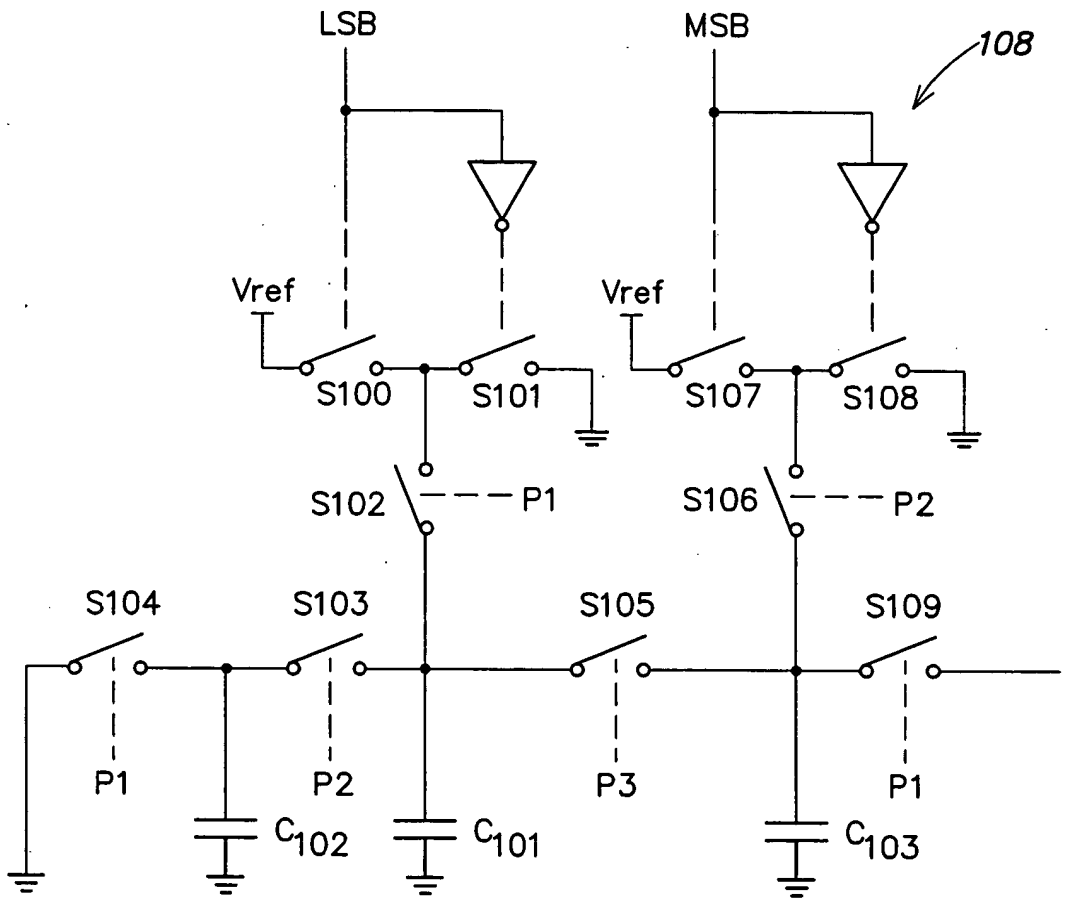

LSB
MSB
108
Vref
Vref
S100
S101
S107
S108
S102
P1
S106
P2
S104
S103
S105
S109
P1
P2
P3
P1
C102
C101
C103

FIG. 18

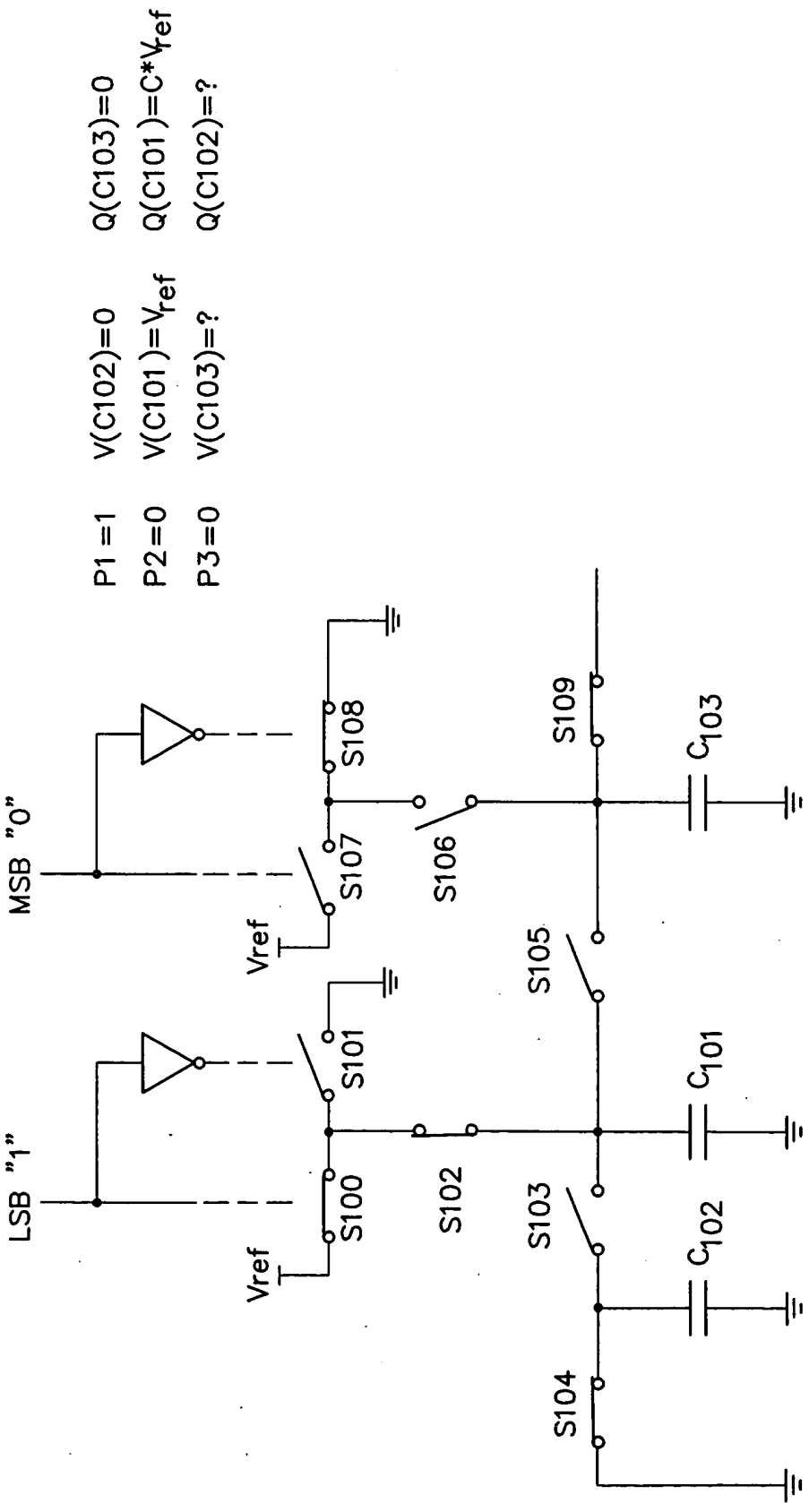

P1 =1
P2=0
P3=0
V(C102)=0
V(C101)=Vref
V(C103)=?
Q(C103)=0
Q(C101)=C*Vref
Q(C102)=?
MSB "0"
LSB "1"
Vref
Vref
S100
S101
S102
S103
S104
S105
S106
S107
S108
S109
C101
C102
C103

FIG. 19A

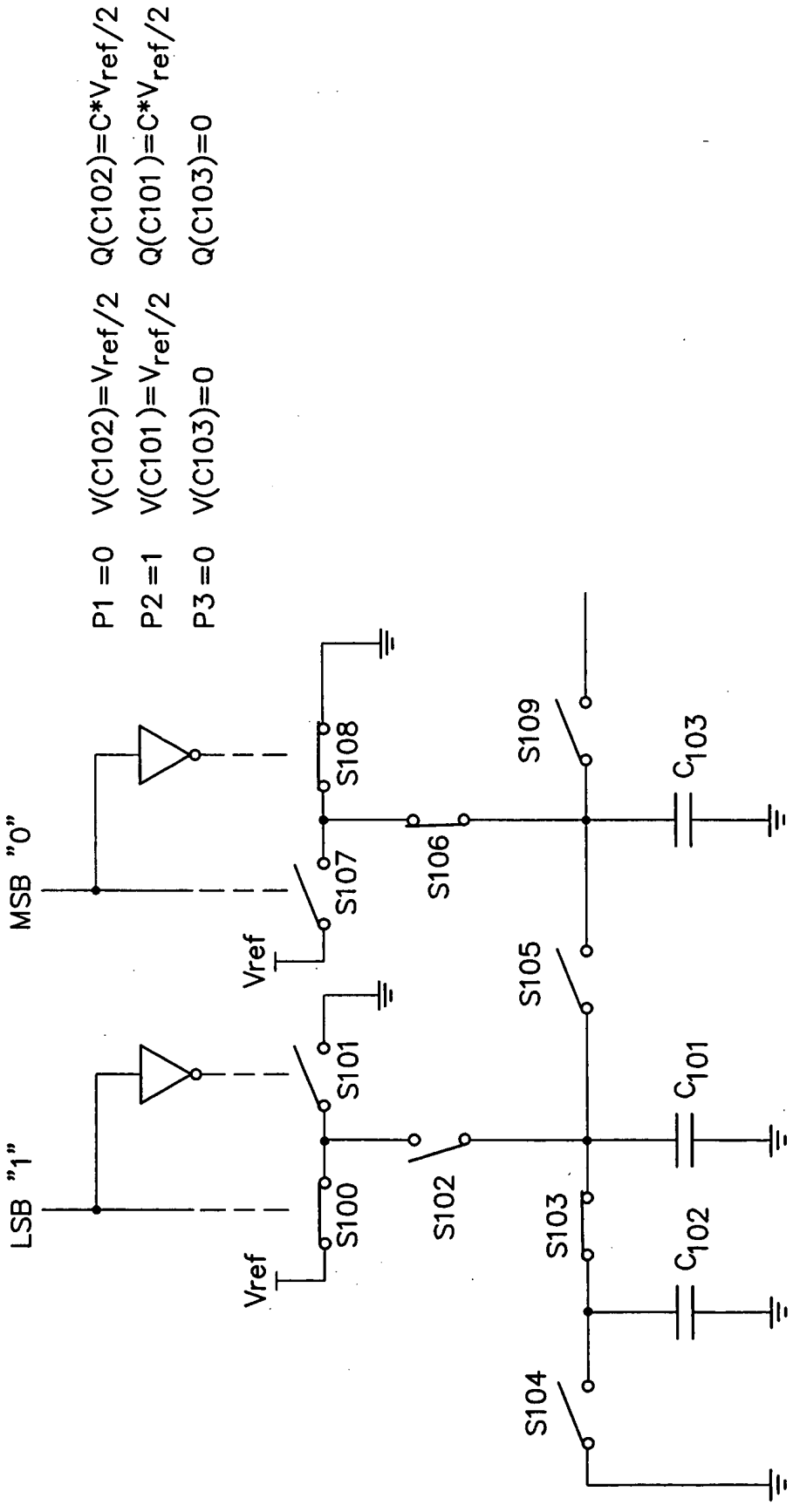

P1 =0 V(C102)=Vref/2 Q(C102)=C*Vref/2
P2 =1 V(C101)=Vref/2 Q(C101)=C*Vref/2
P3 =0 V(C103)=0 Q(C103)=0
MSB "0"
LSB "1"
Vref
Vref
S100
S101
S102
S103
S104
S105
S106
S107
S108
S109
C101
C102
C103

FIG. 19B

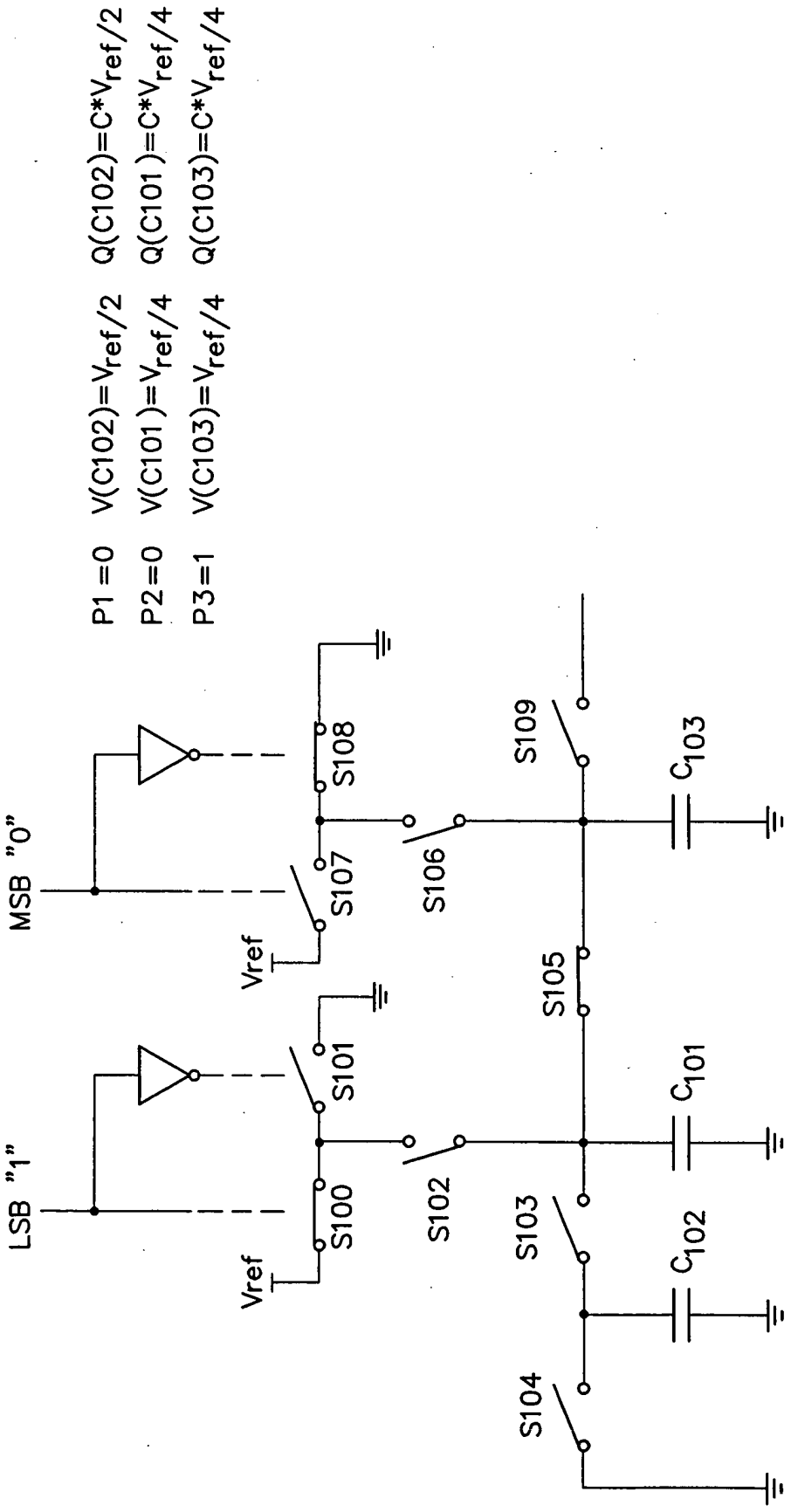

P1 =0 V(C102)=Vref/2 Q(C102)=C*Vref/2
P2=0 V(C101)=Vref/4 Q(C101)=C*Vref/4
P3=1 V(C103)=Vref/4 Q(C103)=C*Vref/4
MSB "0"
LSB "1"
Vref
Vref
S100
S101
S102
S103
S104
S105
S106
S107
S108
S109
C101
C102
C103

FIG. 19C

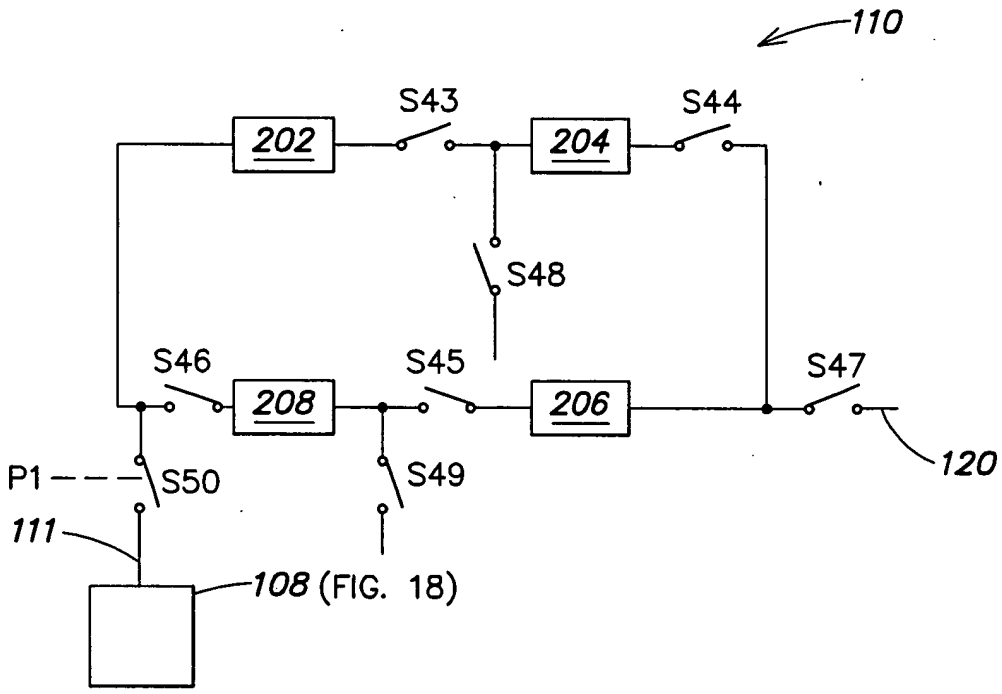

110
S43
S44
202
204
S48
S46
S45
S47
208
206
120
P1
S50
S49
111
108 (FIG. 18)

FIG. 20

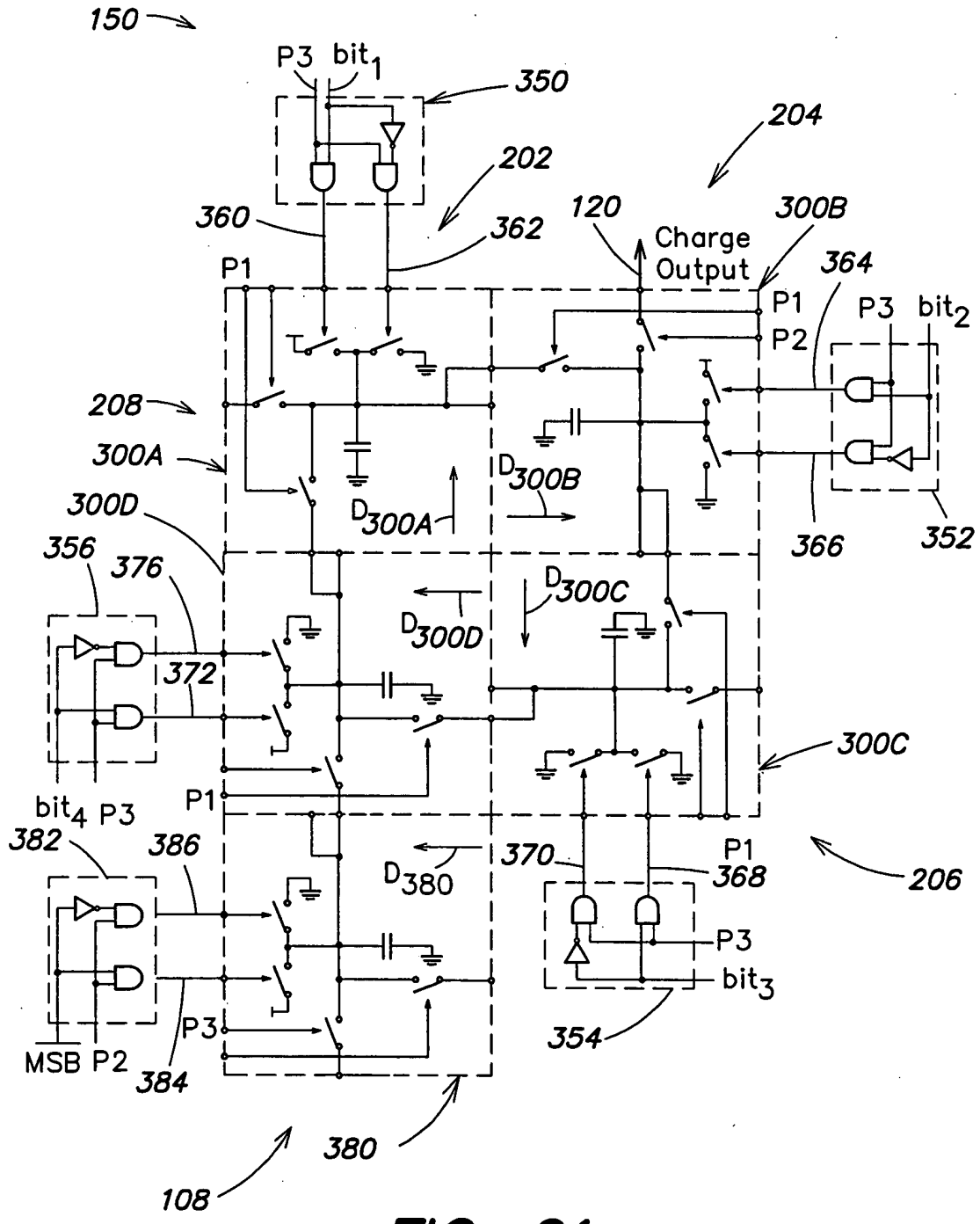

150
P3 bit1
350
204
202
360
362
120
300B
Charge
Output
364
P1
P1
P2
P3 bit2
208
300A
D300B
D300A
300D
366
352
356
376
D300C
D300D
372
300C
bit4 P3
P1
382
386
370
P1
368
206
D380
P3
bit3
MSB P2
P3
384
354
380
108

FIG. 21

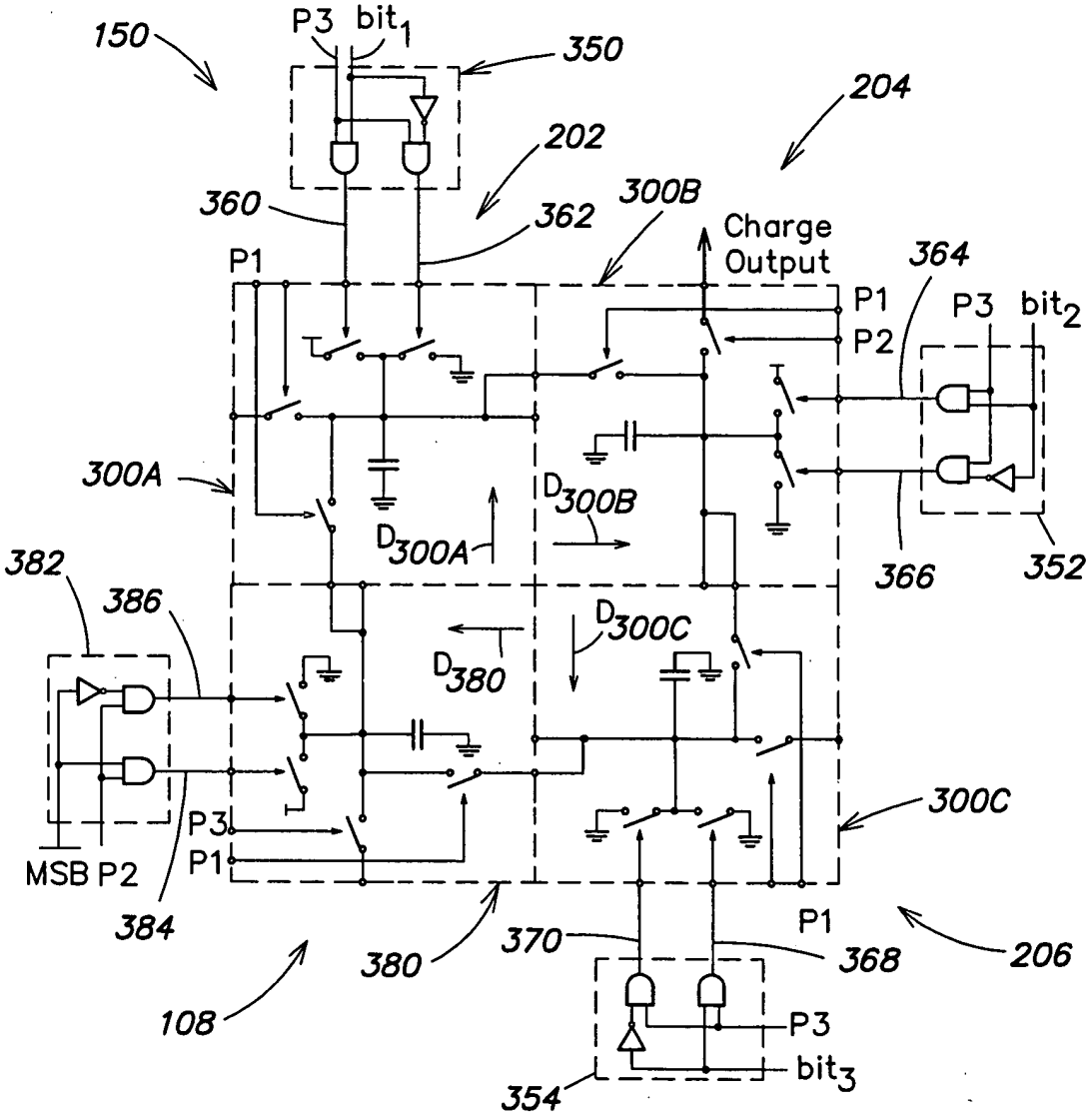

150
P3
bit1
350
204
202
360
362
300B
Charge
Output
P1
364
P1
P2
P3
bit2
300A
D300B
D300A
382
386
366
352
D300C
D380
300C
P3
P1
MSB P2
384
380
370
P1
368
206
108
P3
bit3
354

FIG. 22

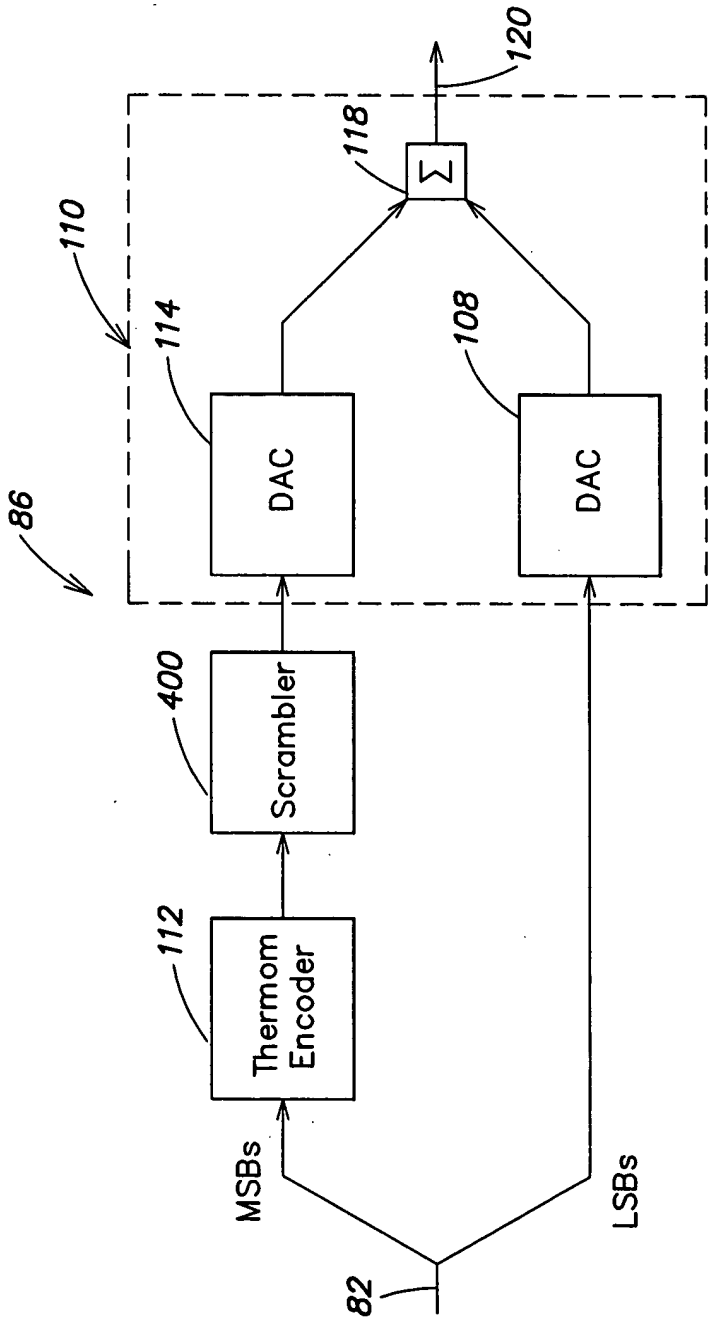

120
118
Σ
110
114
108
DAC
DAC
86
400
Scrambler
112
Thermom Encoder
MSBs
LSBs
82

FIG. 23

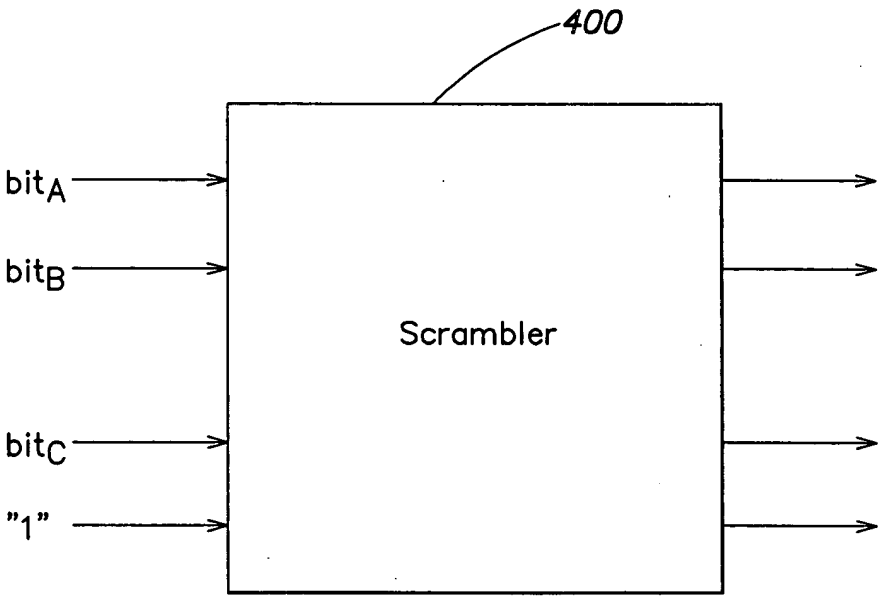


FIG. 24

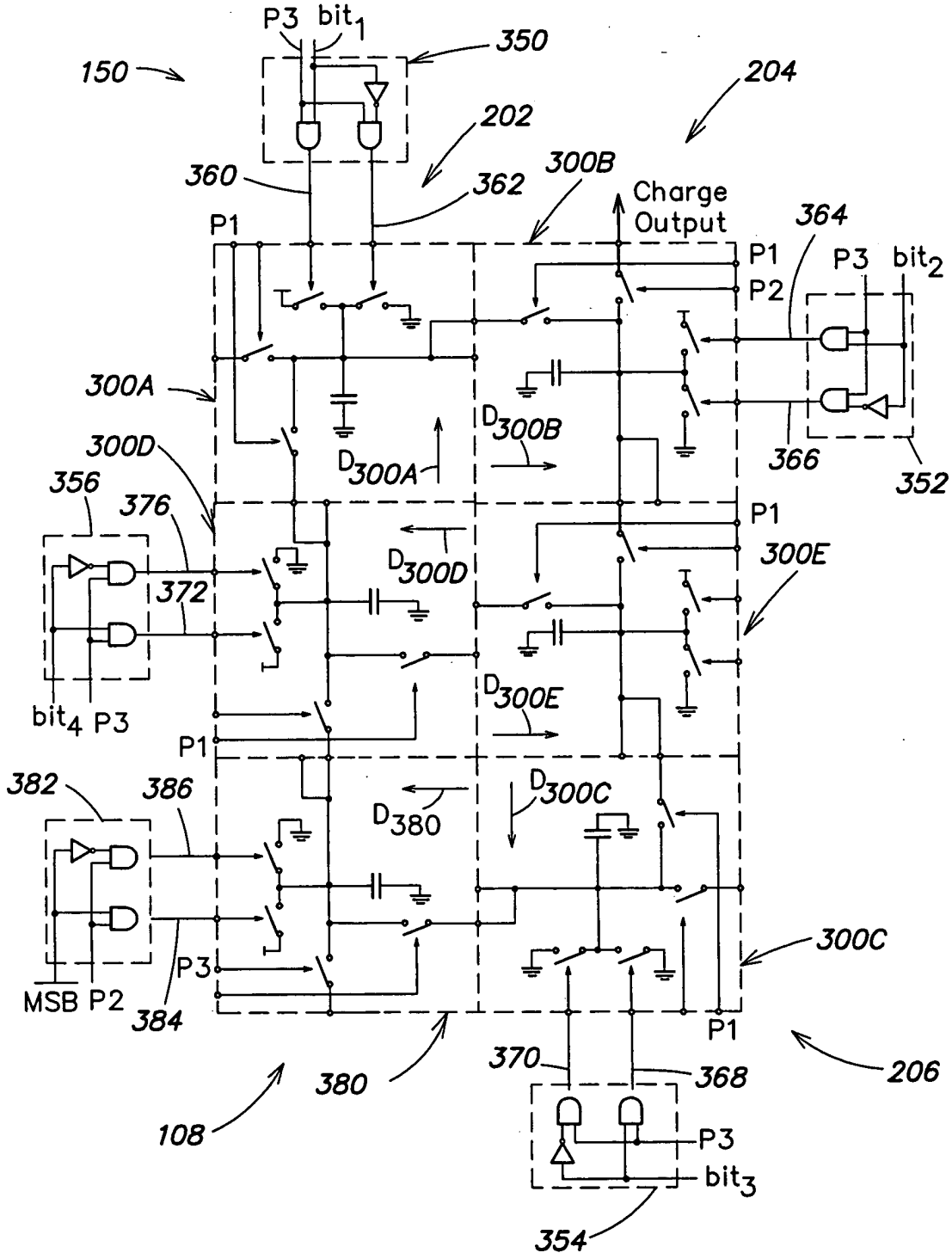

P3 bit1
350
150
204
202
360
362
300B
Charge Output
364
P1
P1
P2
P3 bit2
300A
D300B
D300A
300D
366
352
356
376
P1
300E
D300D
372
D300E
bit4 P3
P1
382
386
D380
D300C
P3
300C
MSB P2
384
P1
206
370
368
380
108
P3
bit3
354

FIG. 25

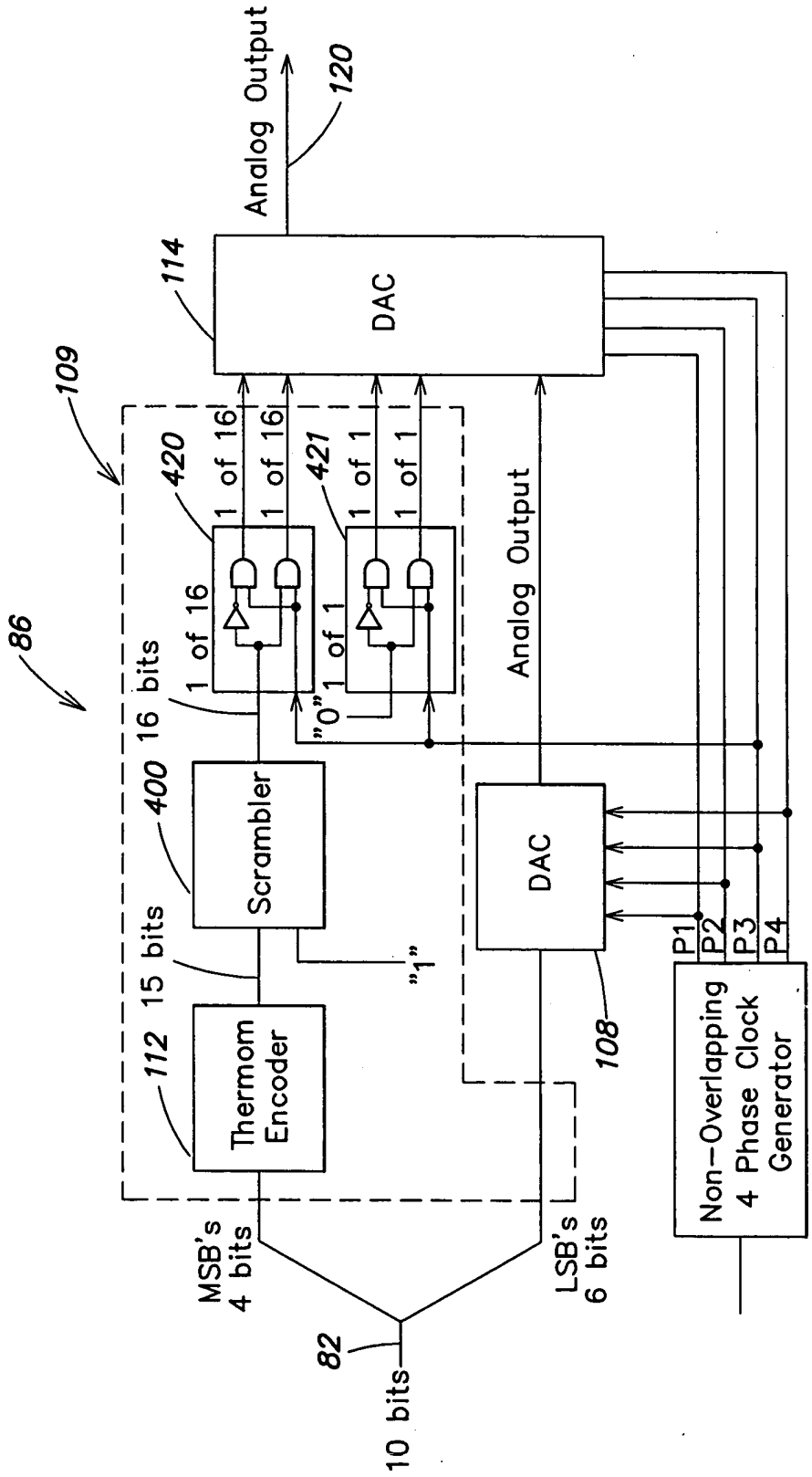

Analog Output
120
114
DAC
109
420
421
1 of 16
1 of 16
1 of 1
1 of 1
1 of 16
1 of 1
"0"
86
16 bits
400
Scrambler
Analog Output
DAC
"1"
15 bits
112
Thermom Encoder
108
P1
P2
P3
P4
Non-Overlapping 4 Phase Clock Generator
MSB's 4 bits
LSB's 6 bits
82
10 bits

FIG. 26

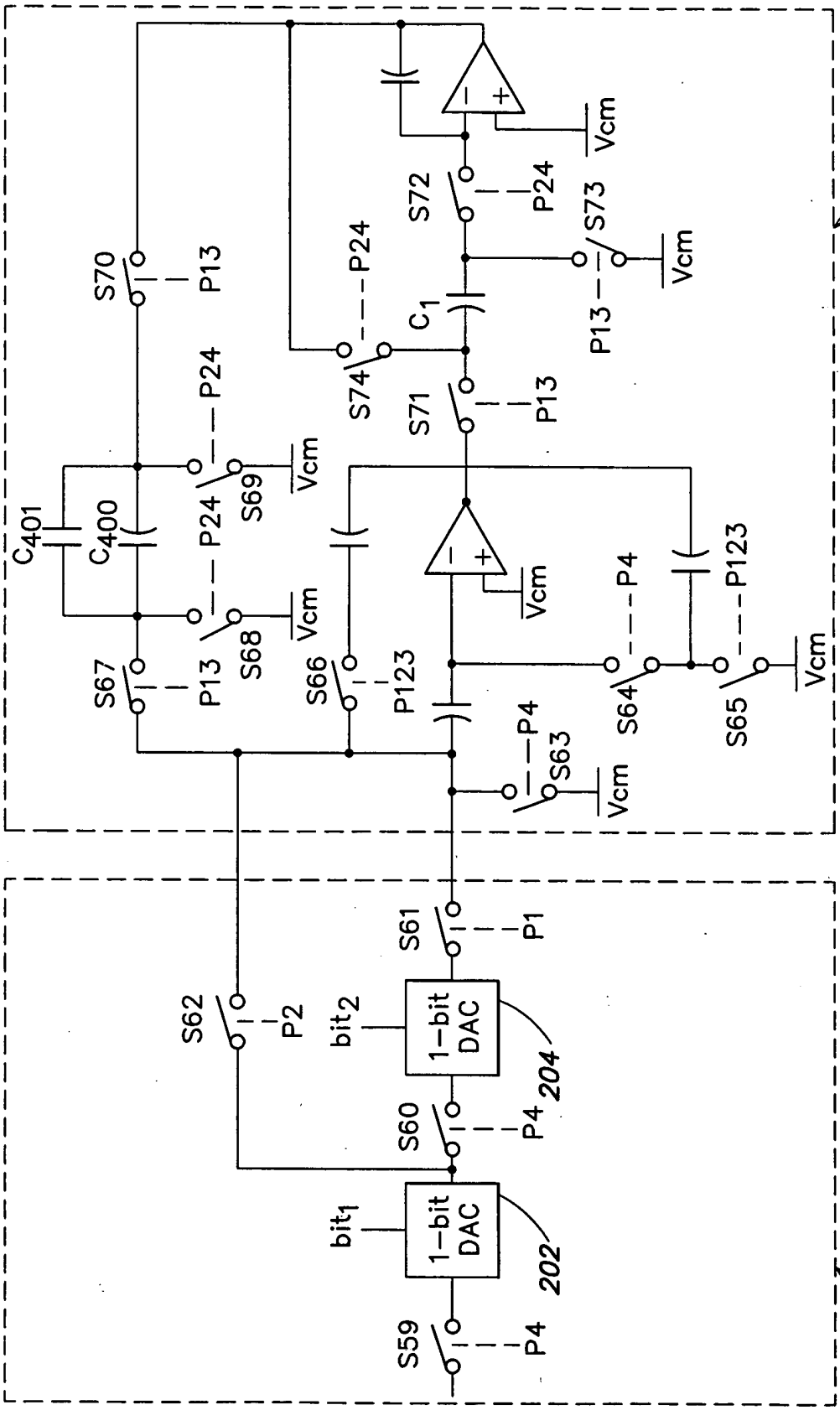

90
86
Vcm
S72
P24
S73
S70
P13
P24
C1
S74
S71
P13
P24
S69
C401
C400
P24
S68
S67
P13
S66
P123
P4
S64
P123
S65
S63
P4
S61
P1
S62
P2
bit2
1-bit DAC
204
S60
P4
bit1
1-bit DAC
202
S59
P4

FIG. 27

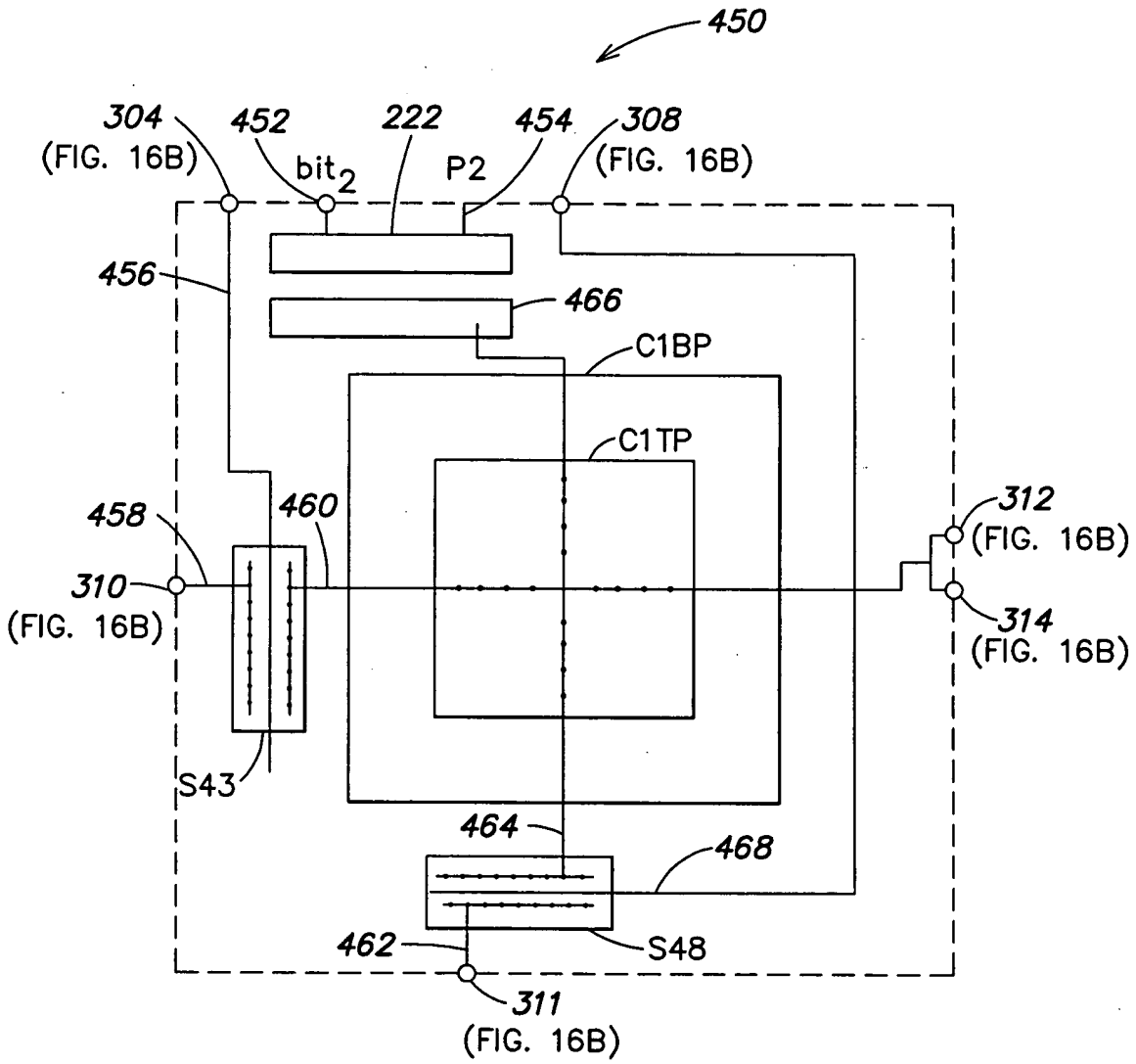

450
304
(FIG. 16B)
452
bit2
222
P2
454
308
(FIG. 16B)
456
466
C1BP
C1TP
458
460
310
(FIG. 16B)
312
(FIG. 16B)
314
(FIG. 16B)
S43
464
468
462
S48
311
(FIG. 16B)

FIG. 28A

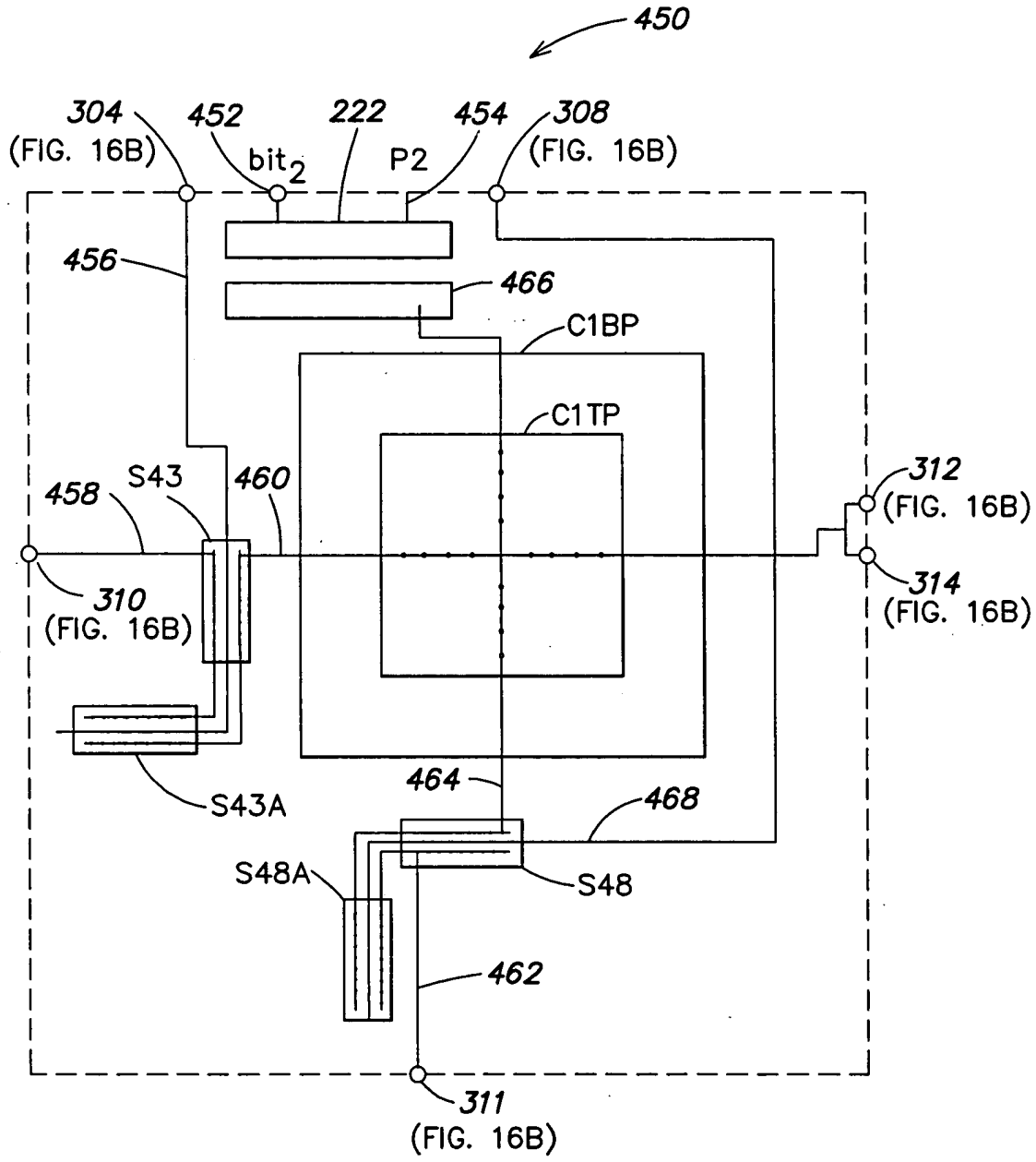

450
304
(FIG. 16B)
452
bit2
222
P2
454
308
(FIG. 16B)
456
466
C1BP
C1TP
458
S43
460
312
(FIG. 16B)
310
(FIG. 16B)
314
(FIG. 16B)
S43A
464
468
S48A
S48
462
311
(FIG. 16B)

FIG. 28B

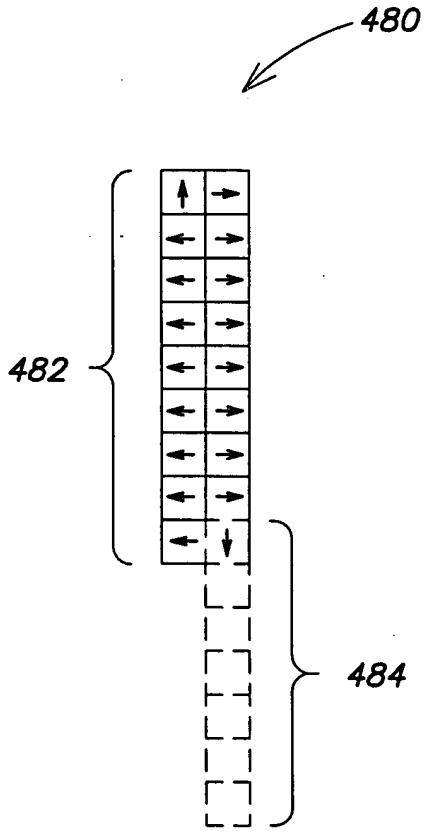


FIG. 29

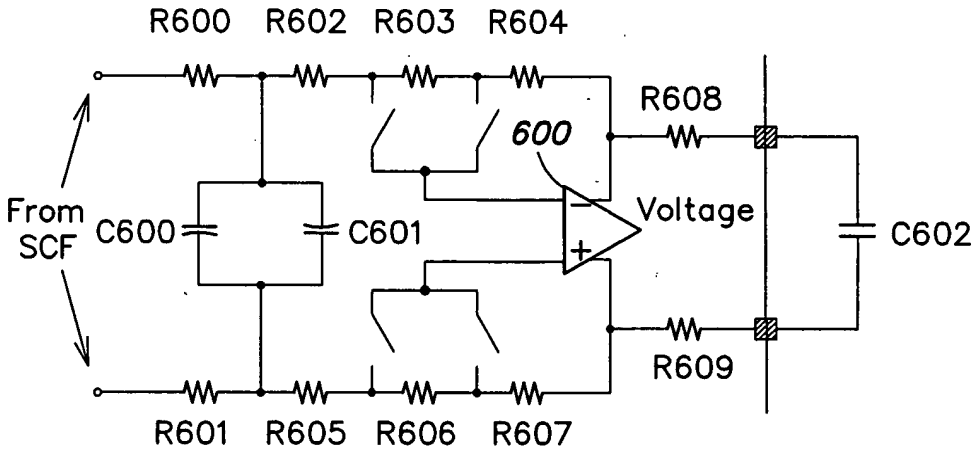

R600
R602
R603
R604
R608
600
From
SCF
C600
C601
Voltage
C602
R609
R601
R605
R606
R607

FIG. 30

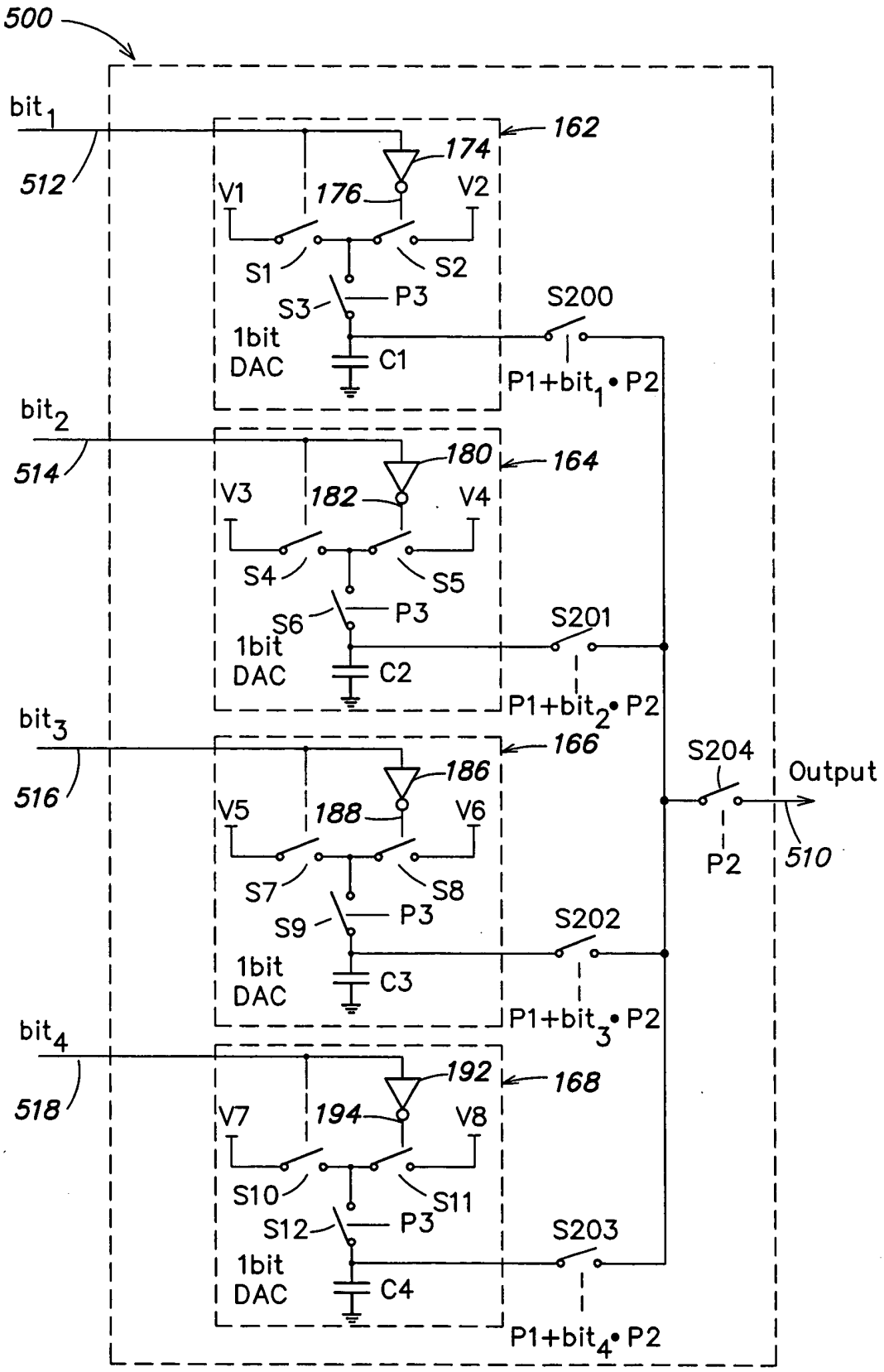

500
bit1
512
162
174
V1
176
V2
S1
S2
S3
P3
S200
1bit
DAC
C1
P1+bit1 • P2
bit2
514
180
164
V3
182
V4
S4
S5
S6
P3
S201
1bit
DAC
C2
P1+bit2 • P2
bit3
516
166
186
V5
188
V6
S7
S8
S9
P3
S202
1bit
DAC
C3
P1+bit3 • P2
S204
Output
P2
510
bit4
518
192
168
V7
194
V8
S10
S11
S12
P3
S203
1bit
DAC
C4
P1+bit4 • P2

FIG. 31

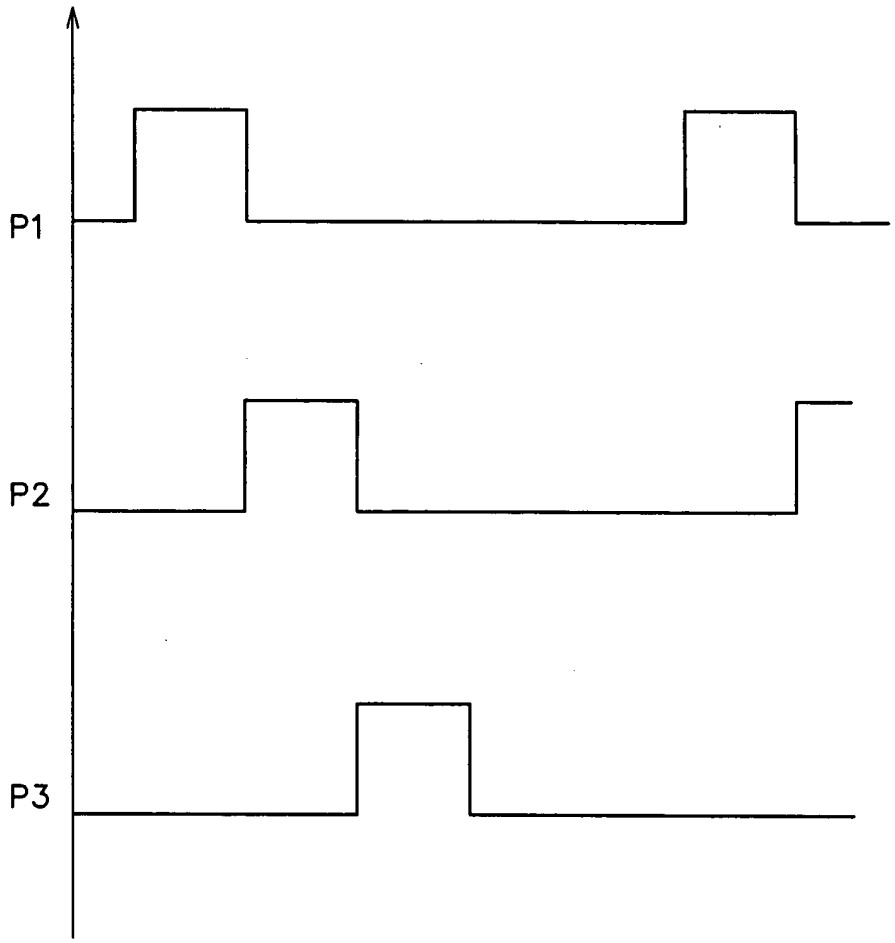
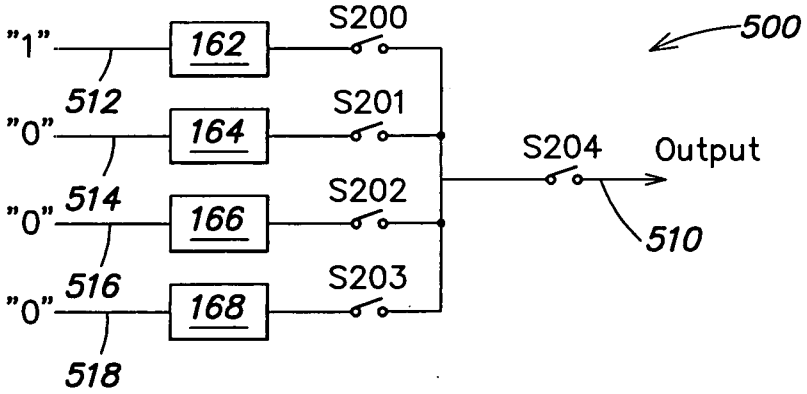
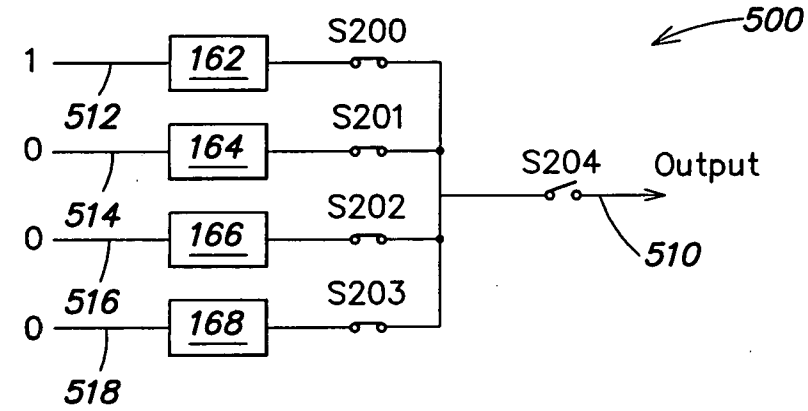


FIG. 32



P1="0"	$V(C1)=V_{ref}$	$Q(C1)=C*V_{ref}$
P2="0"	V(C2)=0	Q(C2)=0
P3="1"	V(C3)=0	Q(C3)=0
	V(C4)=0	Q(C4)=0

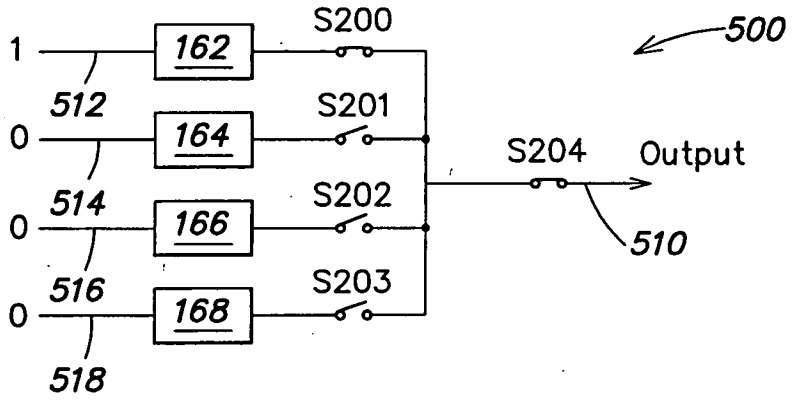
FIG. 33A



P1="1"	$V(C1)=V_{ref/4}$	$Q(C1)=C*V_{ref/4}$
P2="0"	$V(C2)=V_{ref/4}$	$Q(C2)=C*V_{ref/4}$
P3="0"	$V(C)=V_{ref/4}$	$Q(C3)=C*V_{ref/4}$
	$V(C4)=V_{ref/4}$	$Q(C4)=C*V_{ref/4}$

Q delivered to output terminal is $Q(C_1)=C*Vref/4$

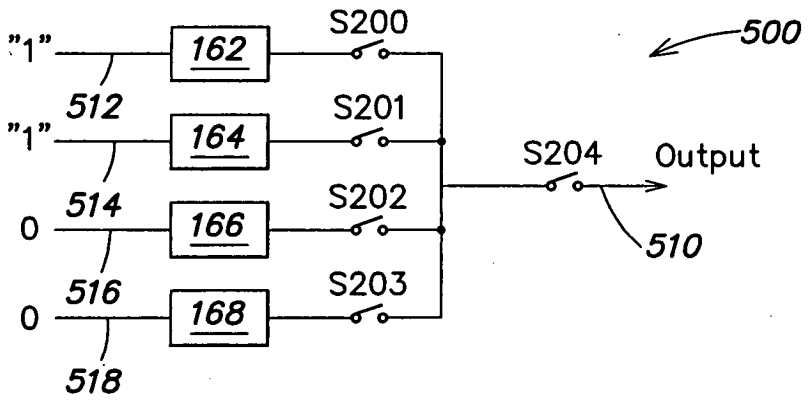
FIG. 33B



P1 ="0"	$V(C1)=V_{ref}/4$	$Q(C1)=C*V_{ref}/4$
P2="1"	$V(C2)=V_{ref}/4$	$Q(C2)=C*V_{ref}/4$
P3="0"	$V(C3)=V_{ref}/4$	$Q(C3)=C*V_{ref}/4$
	$V(C4)=V_{ref}/4$	$Q(C4)=C*V_{ref}/4$

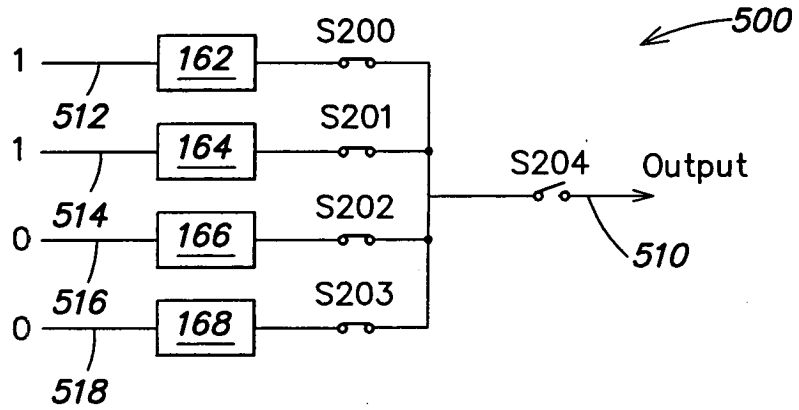
Q delivered to output terminal is $Q(C_1)=C*Vref/4$

FIG. 33C



P1 ="0"	$V(C1)=V_{ref}$	$Q(C1)=C*V_{ref}$
P2 ="0"	$V(C2)=V_{ref}$	$Q(C2)=C*V_{ref}$
P3 ="1"	V(C3)=0	Q(C3)=0
	V(C4)=0	Q(C4)=0

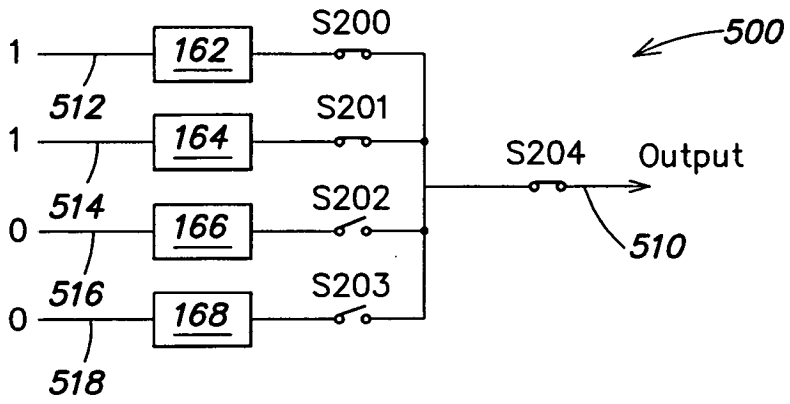
FIG. 34A



P1="1"	$V(C1)=V_{ref/2}$	$Q(C1)=V_{ref/2}$
P2="0"	$V(C2)=V_{ref/2}$	$Q(C2)=V_{ref/2}$
P3="0"	$V(C3)=V_{ref/2}$	$Q(C3)=V_{ref/2}$
	$V(C4)=V_{ref/2}$	$Q(C4)=V_{ref/2}$

Q delivered to output terminal
is $Q(C_1)+Q(C_2)=C*Vref/2+C*Vref/2=C*Vref$

FIG. 34B



P1 ="0"	$V(C1)=V_{ref/2}$	$Q(C1)=V_{ref/2}$
P2 ="1"	$V(C2)=V_{ref/2}$	$Q(C2)=V_{ref/2}$
P3 ="0"	$V(C3)=V_{ref/2}$	$Q(C3)=V_{ref/2}$
	$V(C4)=V_{ref/2}$	$Q(C4)=V_{ref/2}$

Q delivered to output terminal
is $Q(C_1)+Q(C_2)=C*Vref/2+C*Vref/2=C*Vref$

FIG. 34C

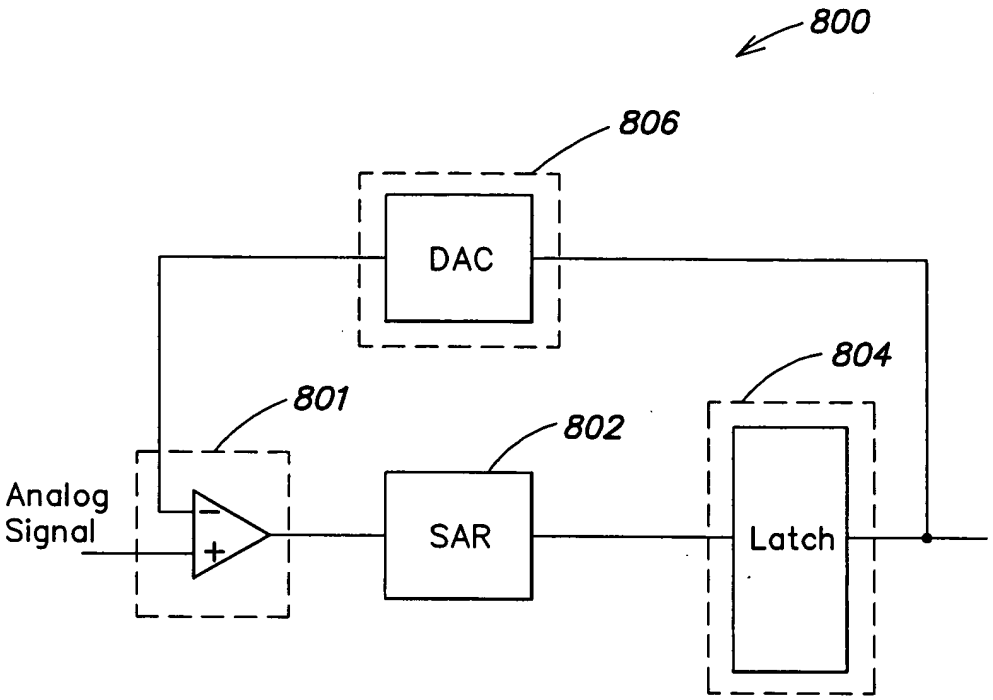


FIG. 35